About The Institute

JNTUA College of Engineering (Autonomous) Ananthapuramu, an esteemed engineering college in Andhra Pradesh was established in 1946 and has been growing continuously in size with respect to intake, faculty strength, number of academic programs offered and infrastructure. It is always committed to offering value-added instruction to widen the horizon of vision for the enrichment of technical education along with skill development. Now it is one of the constituent colleges of Jawaharlal Nehru Technological University Anantapur, Ananthapuramu, Andhra Pradesh.

ATAL Academy:

AICTE Training and Learning (ATAL) Academy is established with the vision "To empower faculty to achieve goals of Higher Education such as access, equity and quality". AICTE is committed for the development of quality technical education in the country by initiating various schemes launched by Govt. of India, Ministry of Human Resource Development. Training is required for increasing the knowledge and skills of students to make them more employable to acquire globalcompetencies.

About The Department

The Department of Electronics and Communication Engineering is established in the year 1974. The Department has come a long way since its inception, keeping pace with the changing needs and expectations of society. The department takes pride in its highly placed alumni all over the globe. The department conducts workshops, symposia, student and faculty development programs regularly to give much-needed exposure to the students and staff on the latest developments in the are of electronics and communication.

About the Programme

The Faculty Development Programme (FDP) on "Exploring the Cutting – Edge world of Chip Design" is a comprehensive training initiative targeting faculty members, researchers, and professionals. The program focuses on providing participants with the knowledge and skills required to design integrated circuits (ICs) from the initial frontend conceptualization to the backend manufacturing phase. Participants gain hands-on experience using industry-standard EDA tools.

Eligibility

Assistant Professors/Associate Professor/Ph.D. scholar's/PG students.

Min/Max Limit- 30/50 participants from the Higher Education Institutions/ Industries.

Mode& Registration

Live class room session in offline mode

Registration has to be done only through https://atalacademy.aicte-india.org/

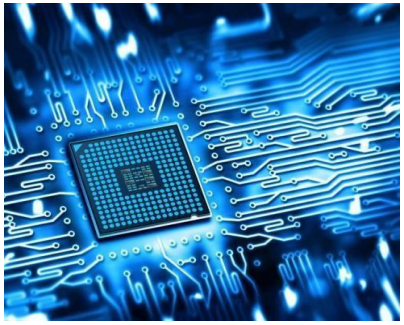
For more information, kindly visit https://aralacademy.aicte-india.org/FAQs

Duration- Six days (Monday to Saturday)

1) 25 hours of teaching in ten equal sessions.
2) 5 hours of practical/labs/ experiential learning sessions of one hour each.
3) 4 hours of article discussion of one hour each.
4) 3 hours, each for MCQs, reflective journal and feedback.
5) 3.5 hours for Industrial visit.

AICTE Training & Learning Academy Faculty Development Programme On Exploring the cutting – edge World of Chip Design

4th – 9th December 2023



Organized by

DEPARTMENT OF ECE
JNTUA College of Engineering (Autonomous)
Ananthapuramu-515002
Andhra Pradesh
www.jntuacea.ac.in

Topics covered

- SoC Design flow and connectivity
- silicon tape out with An emphasis on ASIC SOC/FPGA/IP
- Perspectives of frontend design verification
- System Verilog/UVM,IP/SoC verification
- Validation of FPGA Prototyping
- SoC Verification on FPGA
- Physical Design & Design for testability
- Design preparation for silicon tape out "STA, DTA, synthesis" &netlist generation
- Analog/Mixed Signal IC Design
- NEP 2020

Outcomes

- Enhanced skills and Knowledge on Chip Design.
- This FDP Knowledge helps to update and improve their teaching curriculum to include the latest advancements in chip design.
- Industry - Academia Collaboration strengthen ties between academia and the semiconductor industry, leading to more practical and relevant research and education.
- This FDP helps to engage in innovation & Research in Chip Design.

Requirements to get E-Certificate

- Attendance minimum 80%
- One assessment, combination of MCQs/short answer type/reasoning based, etc.
- 2 Page Article Summary/per Team Teaching Practice – (Individual) - weightage 15 %
- Report/outcome of Industrial visit-(Team) at the last session
- Reflective journal

Resource Persons

PROF. SAMRAT L. SABAT
Designation : Professor
Institution : University of Hyderabad

PROF. SREEHARI RAO PATRI
Designation : Associate Professor
Institution : National Institute of Technology,Warangal

RANGA BABU PEESAPATI
Designation : Associate Professor
Institution : Indian Institute of Technology, Design and Manufacturing, Kurnool

ARJUN NAG
Company : Tata ConsultancyServices
Designation: Senior Design verification lead

DEVARAJU RAGHAVENDRA
Company : Intel
Designation: SOC design engineer

V B CHITHRA
Designation : Professor
Institution : JNTUA College of Engineering,Anantapur

PRADEEP KATIKILA
Company : Craftronics
Designation : Senior Application Engineer

Prof. G. RANGA JANARDHANA

Vice Chancellor, JNTUA, Ananthapuramu

Patron

Prof. M. Vijaya Kumar

Rector, JNTUA.

Prof. C. Sashidhar

Registrar, JNTUA

Co-Patron

Prof. V. Satya Narayana

Principal, JNTUA

Coordinator

Dr. G. Mamatha

Assistant Professor in ECE

Co-Coordinator

Dr. S. Chandra Mohan Reddy

Professor & HOD in ECE

Contact Details:

Dr. G. Mamatha
Assistant Professor in ECE
e-mail: gmamatha.ece@gmail.com
Contact No:9490446399