



## ABOUT INSTITUTION :

Santhiram Engineering College (Autonomous) is sponsored by M/s Sri Shirdi Sai Educational Academy, Nandyal. SREC is established under the able guidance of Dr. M. Santhiramudu, Chairman, in the year 2007 with a noble motto "Education for Peace and Progress".

### Highlights of the College:

- Received Autonomous Status.
- Accredited by NBA for the Departments of ECE and CSE.
- Accredited by NAAC with Grade-A (3.2 score)
- Recognized as Q-Mentor College by APSICHE, for guiding HEIs for accreditation.
- Listed as one of the Best Engineering College with AA+ Grade by Career 3600 in the year 2023.
- Recognized in GOLD CATEGORY by AICTE-CII Survey for the years 2017 & 2018 and also in PLATINUM CATEGORY in the year 2020.
- Received TWO University Gold Medals from JNTUA, Ananthapuramu.
- Received NINE Prathibha Awards from the Govt of A.P.
- SIX Patents were granted and SIX patents were approved under AICTE-KAPILA Scheme.
- Received around 50 Lakhs worth of funding projects under various schemes of UGC, AICTE, IEEE, IE and etc.

### SREC VISION:

To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.

### SREC MISSION:

- To provide Advanced Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization by arising a self-sustained University.
- To establish postgraduate programs in the current and Advanced Technologies.
- To establish an R&D Consultancy through developing Industry Institute Interaction, building up exceptional infrastructure.
- To propel every individual, realize and act for the technical development of the society.

### Chief Patron

**Prof. G. Ranga Janardhana**  
Hon'ble Vice-Chancellor, JNTUA

### Patrons

**Prof. M. Vijaya Kumar**  
Rector, JNTUA  
**Prof. C. Sashidhar**  
Registrar, JNTUA

### Program Director

**Prof. B. Esvara Reddy**  
Director, Faculty Development Cell, JNTUA. Secretary, ISTE AP Section

### Chair Persons

**Dr.M.Santhiramudu**  
Chairman, SREC  
**Er.M.Siva Ram**  
MD, SREC

### Principal

**Dr. M.V.Subramanyam**  
Principal, SREC

### HOD-ECE

**Dr.Y.Mallikarjuna Rao**  
Professor, SREC

### Program Coordinator

**Dr.G.Sowmya**  
Dean-R&D, SREC

**Contact: 9441401197**  
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### Organizing Committee

**Dr.C.Shivanath Chaudhri,**  
Assoc.Prof, SREC  
**Dr.B.Divya Madhuri,**  
Assoc.Prof, SREC  
**Ms.B.Alekya Himabindu,**  
Asst.Prof, SREC



## Five Day Faculty Development Program on

## Recent Trends in VLSI Technologies and Practical Approaches towards IP Using EDA Tools

**October 09-13, 2023**

**Organized  
by**

**Dept. of Electronics &  
Communication Engineering**

**SANTHIRAM ENGINEERING COLLEGE**  
(Autonomous)

Approved by A.I.C.T.E., New Delhi, Permanently Affiliated to JNT University, Ananthapuramu  
Accredited by NAAC with Grade-A, Accredited by NBA (ECE & CSE)  
An ISO 9001:2015 Certified Institution, 2(f) & 12(B) recognition by UGC Act, 1956  
NH-40, NANDYAL-518501 (Dist), A.P.  
www.srecnandyal.edu.in

and

**Faculty Development Cell  
Jawaharlal Nehru Technological University  
Ananthapuramu ( JNTUA)**

**In association**

**with**

**ISTE AP Section**



# 5 Day FDP on Recent Trends in VLSI Technologies and Practical Approaches towards IP Using EDA Tool

## Resource Persons

- Dr.P.ChandraSekhar,  
Professor, Department of ECE, OU, Hyderabad
- Dr.B Chenna Reddy,  
Verification Engineer, AISemiCon, Bangalore
- Dr.K Vasudeva Reddy,  
Member of Technical Staff, IP& Design Engineering,  
GlobalFoundries, Bangalore
- Dr.Manoj Kumar Majumder,  
Assistant Professor, ECE, IIIT-NR
- Mr. N.Nageswara Reddy,  
Senior engineer-AMS design, CYIENT Pvt Ltd,  
Hyderabad.
- Dr. Mamidi Nagaraju,  
Technical Manager at Entuple Technologies.

## About FDP

An intensive one-week sponsored faculty Development programme is being organized for faculty of engineering and technological institutions. It is also open to persons from industry, doctoral students and faculty from different organizations.

This faculty development programme (FDP) is devoted to addressing the need to enhance the knowledge about the latest technologies pertaining to Recent Trends in VLSI Technologies and Practical Approaches towards IP Using EDA Tools is being conducted at Santhiram Engineering College Nandyal under the sponsorship of JNTU Ananthapuramu. The whole course is handled by and professors from different IIT, NIT and Industry experts.



Scan to Register

<https://forms.gle/CbCPVdcnuhPbSX9g8>

## Session Topics:

**Session 1:** Introduction and recent trends in VLSI technologies

**Session 2:** Brief on Bluetooth and IoT receivers

**Session 3:** Low noise amplifiers for RF and mm Wave applications using SOI technology

**Session 4:** LCVCOs for RF and mm Wave applications using SOI & bulk CMOS Technology

**Session 5:** Deep dive into digital fundamentals (Industry perspective)

**Session 6:** ASIC and verification flow- Design perspective

**Session 7:** Introduction on Power management IC (PMIC)

**Session 8:** Design of Op Amp & Band gap Reference circuit

**Session 9:** Low drop out (LDO) Regulators- Design tradeoffs

**Session 10:** DC-DC converters-Variou flavors and their designs

**Session 11:** Practical sessions using cadence Virtuoso (two stages Op Amp)

**Session 12:** Practical sessions using cadence Virtuoso (Band gap Reference)

## Objective:

- To train the faculty in the important area of industrial relevance through academic and industrial experts
- To provide hands on experience on the usage of various tools, models, methodologies and techniques
- To provide comprehensive idea of various industrial best practices in the field and make them adapt in their academic curriculum as case studies
- To emphasis the pedagogy of learn by doing with exposure to the state of the art commercial tool for verification purpose
- To provide training on Cadence EDA tools.

## Expected Outcome:

By the end of the faculty development program, the participants got an overall idea about VLSI design creation using the Cadence EDA tool.

## Important Dates:

Last Date for Registration : 05-10-2023  
Intimation of Selection : 07-10-2023  
Confirmation by the Participants : 08-10-2023  
Program Duration : 09-10-23 to 13-10-23

## Registration :

- No Registration Fee
- Faculty / Ph. D Scholars of Electronics & Communication Engineering / Allied disciplines are eligible to attend the program.
- Participants will be selected on First-Come & First-Serve basis.
- Number of registrations limited to 25-30
- Participants are advised to bring their own laptops for practice.
- Accommodation will be provided for outstation participants on prior request.

## Participation Certificate:

Certificates will be issued based on the attendance percentage and submission of feedback.