Department of Electronics & Communication Engineering
JNTUA College of Engineering (Autonomous), Ananthapuramu

5 - Day Online Training Program on "ASIC Front End Design & Verification"
Sponsored by TEQIP-III

Date : 21st to 25th September 2020
Registration Link : https://rb.gy/nmm89z

About the College

JNTUA College of Engineering (Autonomous) Ananthapuramu, an esteemed engineering college in Andhra Pradesh was established in 1946 and has been growing continuously in size with respect to intake, faculty strength, number of academic programs offered and infrastructure. It is always committed to offer value added instruction to widen the horizon of vision for the enrichment of Technical education along with skill development.

About the Department

The department of Electronics and Communication Engineering is established in the year 1974. The department has come a long way since its inception, keeping pace with the changing needs and expectations of the society. At present, the department is running a full time UG program in Electronics and Communication Engineering, three PG programs in Digital Electronics & Communication Systems (DECS), VLSI System Design and Internet of Things specializations. The department conducts workshops, symposia, student and faculty development programs regularly on latest developments in the area of electronics and communication.

About Collaborating Partner - Entuple Technologies

Entuple is a next generation solutions enabler in cutting edge technologies. Entuple delivers world class simulation solutions in Applied Electromagnetics, Semiconductor (VLSI), System Design & Reliability, Mechanical, CFD and RF. Entuple has developed its own range of semiconductor based power drives and process control solutions. They cater to wide range of customers in semiconductor, manufacturing, defense & aerospace and academia.

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Objective of the Program

VLSI technology has gone through rapid strides in last few decades. Designing efficient systems continuous to get more and more complex due to ever increasing demand for power, area and cost-effective solutions in digital and analog IC design. Understanding the importance, this online training program is aimed and designed keeping in mind the need of UG/PG Students as well as PhD Scholars and faculty members who are working in this area. This training program shall cover both theoretical as well as the demo sessions which will give good exposure to the participants on front end design and verification of digital systems. Various applications/case studies would also be covered.

Eligibility

Faculty/Research Scholars/UG & PG Students of ECE and allied branches are Eligible to apply.

Program Schedule

Date	Morning Sessions	Afternoon Sessions
21st Sep	Overview of VLSI, ASIC, FPGA flow – Industry Perspective	Getting started with Digital Design: Modeling & Simulation – DEMO
22nd Sep	Digital Design Stages, Modeling using Verilog	Design of Combinational Logic circuits using Verilog
23rd Sep	Modeling of Sequential Logic Circuits – Guidelines	Sequential Logic Circuits Modeling and Simulation – DEMO
24th Sep	Design of State Machines, Memories & Functional Verification	Protocol Verification: AMBA APB Protocol – Project Case Study Discussion
25th Sep	Protocol Verification: AMBA APB Protocol, Low Power Design Techniques	Design of State Machines – Project Case Study Discussion

CONVENER

Prof. P Ramana Reddy
Head, Department of ECE
JNTUA CEA

CO-PATRON

Prof. P Sujatha
Vice-Principal
JNTUA CEA

PATRON

Prof. K Govinda Rajulu
Principal
JNTUA CEA

CO-ORDINATORS

Dr. V. Sumalatha
Professor, Department of ECE
JNTUA CEA

Dr. G Mamatha
Asst. Professor, Department of ECE
JNTUA CEA

There is NO Registration Fee &
Last Date to Resister - 19th September 2020

Contact details for any Queries:
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RESOURCE PERSONS

1. Damodara M S, Business Head with 19 years of Industry experience
2. Shivappa K M, Director with 22 years of Industry experience
3. Navin Sankar, Sr. Design Engineer with 8 years of experience in VLSI domain
4. Avinash Keshav, Sr. Application Engineer with 7 years of experience in VLSI industry

INSTRUCTIONS TO PARTICIPANTS

- Link for the online Platform will be sent to the Registered Candidates Email ID.
- Attendance of 100% is compulsory for E-certification.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

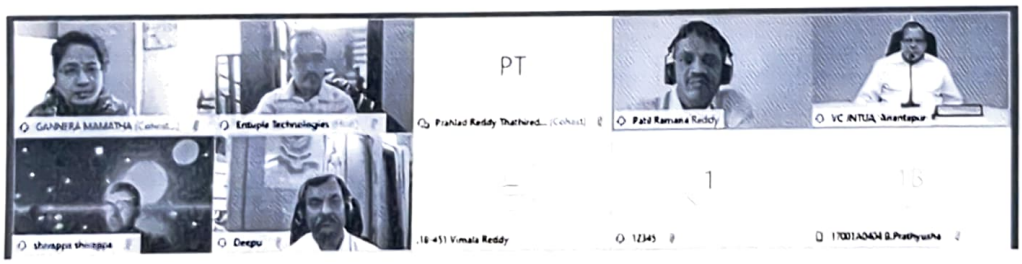
Five–Day online Training Program on " ASIC Front End Design &Verification"

21 to 25 of September, 2020

Sponsored by TEQIP-III

REPORT

The department of Electronics and Communication Engineering has successfully organized a five-day workshop on the subject "ASIC Front End Design & Verification" in association with Entuple Technologies, Bangalore. The main objective of this 5 day program is to provide exposure to the participants on digital design and verification aspects of ASIC. The term ASIC stands for Application Specific Integrated Circuit. It is an integrated circuit customized for a particular use, rather than intended for general-purpose use. This designing supports the development of embedded systems. In the recent years, there has been a significant increase in the demand for chip driven products especially for ASICs in consumer electronics, medical electronics, communication, aero-space, computers and many other sectors.



On 21st[th]of September, the event began with the inaugural function at 9:30AM with University Invocation song. Prof S Srinivas Kumar has acted as chief guest and presented his views on the importance of VLSI, LOW Power VLSI and Image Processing for the students career point of view. He has invited industries to collaborate with the University for Knowledge gaining for both faculty and students and also encouraged multi disciplinary course incorporation in the University for the Students Benefit. Prof. K. Govidarajulu principal of the college, Prof. P. Ramana Reddy, Head of the Department, Mr. Damodaram M.S, Business Head, Entuple Technologies Pvt. Ltd., coordinators Prof. V. Sumalatha and Dr. G. Mamatha were present at the event.

Workshop – Day 1

Forenoon:

The morning session was taken over by Mr. K M Shivappa, who is the industrial expert at VLSI design. He is a 22 year experienced, very high-profile- senior design engineer at Entuple Technologies, Bangalore.

It started with a power point presentation on their work at Entuple Technologies and their

leading presence in Design and Verification using Verilog. It was continued with the explanation of Overview of VLSI, ASIC flow, FPGA flow – Industry Perspective.

Afternoon:

The Cadence tool – Incisive Enterprise Simulator is briefed in detail by the resource person and hands-on designing of the basic AND gate as an design is explained to the students using a online meeting application Cisco-Webexby Mr. M S Damodara who has 19 years of industry experience

Workshop – Day 2 Forenoon:

The second day was initiated by Mr.M S Damodara who has 19 years of industry experience started with the basics of Digital Electronics like Number system , Logic gates , Realization of gates, Combinational Circuits and their application problems also basics of Verilog Language how to write and compile the Design written in Verilog language explained with a Power point presentation to the students using a online meeting application Cisco-Webex

Afternoon:

The afternoon session initiated by Mr.Naveen Sankar who has 8 years of industry experience started with designing of a simple Logic circuit using basic gates as instances for the design. This was took upto explain the Design by Writing a Verilog language for that instance and a basic thing that need to be kept in mind while writing the verilog code for the Design. Also guided in how to write a Test bench code for the Design to verify according to our specifications required.

The final written verilog code in Cadence – IES (Incisive Enterprise Simulator) was simulated and checked for any errors in the code. Upon successful simulation the variables are added to the Simvision which shows the output waveform for a simulated Design Code. Also explained with two more examples to students so that they can have a clear perspective of the Design and verifying the code.

Workshop –Day 3

Forenoon:

The third day started with Mr. AvinashKeshav , application engineer with 7 years of experience in VLSI industry demonstrated about Sequential Circuits , how they are designed and their mode of operation and their role in Designing Circuits .Explained about flipflops, counters ,registers and their necessity in the Design perspective through online meeting application Cisco-Webex.

Afternoon:

The afternoon session started with the designing of sequential Circuits their Design modeling and Simulation using Verilog language . Explained through an example like flipflops ,designed its code and written a testbench code for it to verify according to our specifications simulated the design and added the design variables to the Simvision to observe the output waveform in Cadence –IES. Also explained sequential Modeling and simulation by considering two more examples.

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Workshop – Day 4

Forenoon:

The fourth day started with Mr. AvinashKeshav , applicationengineer with 7 years of experience in VLSI industry demonstrated about the design of State Machine and their role in present day applications of the Design. Explained about Moore and Mealy Machines by considering one example also explained the transition of bits to the another state depending on two types of sequences like Overlapped sequence and Non-Overlapped sequence and their differences .Also explained the difference between Moore ,Mealy state Machine.

Explained about Memories like RAM,ROM and their classification based on storage capacity and also about SRAM and DRAM and their circuit specifications and also their mode of operations and also about the Functional Verification

Afternoon:

The session was initiated by Mr. M S Damodara who has 19 years of Industry experience demonstrated about AMBA APB Protocol , its significance in Designing a hardware and its operation . APB protocol is a Advance Peripheral Bus protocol which is used for bulk transfer of address, data , control signals to its peripherals connected and its operation how the data transfer occurs , handshaking process, reading the data , writing the data, and control signals and their transactions in a Bus architecture.

Workshop – Day 5

Forenoon:

The session was started with the APB protocol review a small recap by Mr.Avinash Keshav , application engineer with 7 years of experience in VLSI Industry . Explained APB protocol Verification how it does in an effective manner . And then started an another important topic Low Power Design Techniques – Now a days as the technology is advancing effectively there must be a low power consumption and less leakage power in an Design ,with this advanced technology in VLSI Industry every Design must have a low power consumption and also it is a tradeoff between speed and time and explained a those techniques very effectively.

Afternoon:

The session was held by Mr. M S Damodara, also shared their knowledge on power reduction techniques smoothly and also clarified the doubts of every student very peacefully and clearly .Also on request on students executed two more verilog design codes with a neat picture of design . Explained the State Machine case study by considering an example of both Overlapping and Non-Overlapping Sequences. At last there was a feedback from the students in a positive response regarding the 5 day online training program and how it helped them in this pandemic situation and had gained the knowledge how the VLSI Industry is Emerging towards the new accomplishments made by an Engineer

Online training program was ended with the token of gratitude note by Prof. V.Sumalatha and Dr. G. Mamatha to Mr. M S Damodara, and also entire Entuple team who has been here all the while monitoring students and making sure that they had gained knowledge on VLSI–Industry Perspective.

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TEQIP III

Certificate of participation

ENTUPLE TECHNOLOGIES

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) ANANTHAPURAMU

5 DAY ONLINE TRAINING PROGRAM ON

ASIC Front End Design & Verification

SPONSERED BY **TEQIP III**

This is to certify that Dr./Mr./Ms **Mamatha** has participated in 5 day online training program on "**ASIC Front End Design & Verification**" during 21st to 25th September 2020

CO-ORDINATOR	CO-ORDINATOR	CONVENER	PATRON
Dr. G Mamatha	**Prof. V Sumalatha**	**Prof. P Ramana Reddy**	**Prof. K Govinda Rajulu**
Asst. Professor, ECE	Professor, ECE	Head, Department of ECE,	Principal,
JNTUA CEA	JNTUA CEA	JNTUA CEA	JNTUA CEA

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