PROCEEDINGS OF THE PRINCIPAL, JNTUA COLLEGE OF ENGINEERING ANANTHAPURAMU (AUTONOMOUS) : JNTUACEA ANANTHAPURAMU
PRESENT : Prof. K. GOVINDA RAJULU : PRINCIPAL

TEQIP-III

Procs. No. TEQIP-III/NPIU/Academics/1.3-2(iv)/33/2020-21 Date: 17/09/2020

Sub: JNTUACEA – TEQIP-III – Academics – Permission to conduct Online Five day Training Program on "ASIC Front End Design & Verification" for UG/PG Students, Research Scholars and Faculty Members at JNTUACEA during 21-25 September, 2020 – Orders – Issued.

Ref: Letter Dt: 14-09-2020 from Prof. V.Sumalatha and Dr. G.Mamatha, Asst. Prof., Dept. of ECE, JNTUACEA.

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Prof. V.Sumalatha and Dr. G.Mamatha, Asst. Prof., Dept. of ECE, JNTUACEA has submitted a letter requesting the Principal for permission to conduct Online Five day Training Program on "ASIC Front End Design & Verification" for UG/PG Students, Research Scholars and Faculty Members at JNTUACEA during 21-25 September, 2020 and requested to meet the expenditure from TEQIP-III funds.

Title of the Programme	ASIC Front End Design & Verification
Conducted at	**JNTUACEA**
Dates of Training	**21-09-2020 to 25-09-2020**
Co-ordinator's	**Prof. V.Sumalatha, Dept., of ECE** **Dr. G.Mamtaha, Asst. Prof., Dept. of ECE,**

The requisition submitted is approved and the Principal is pleased to accord permission to Prof. V.Sumalatha and Dr. G.Mamatha, Asst. Prof., Dept. of ECE, JNTUACEA to conduct the above said programme on the date(s) noted. The expenditure will be met from TEQIP-III funds under Academics SC 1.3-2(iv) head of account.

It is requested to follow the rules and regulations in incurring the expenditure and requested to submit the vouchers in original as per the guidelines provided by NPIU. And also requested to submit Photographs, list of participants, reports etc., as per TEQIP-III norms in Performa provided.

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To

Copy to Prof. V.Sumalatha and Dr. G.Mamatha, Asst. Prof., Dept. of ECE,
Copy to Dr.K.Madhavi, TEQIP-III Co-ordinator & Nodal Officer (P)
Copy to Prof.P.Sujatha, Vice Principal, Nodal Officer (A) (TEQIP-III)
Copy to Dr.K. Jithendra Gowd, Nodal Officer (F) & TEQIP MIS officer
Copy to Bills.

PRINCIPAL
J.N.T.U.A. College of Engg.
(Autonomous)
ANANTHAPURAMU 515002
A.P. INDIA

Received
G Mamatha

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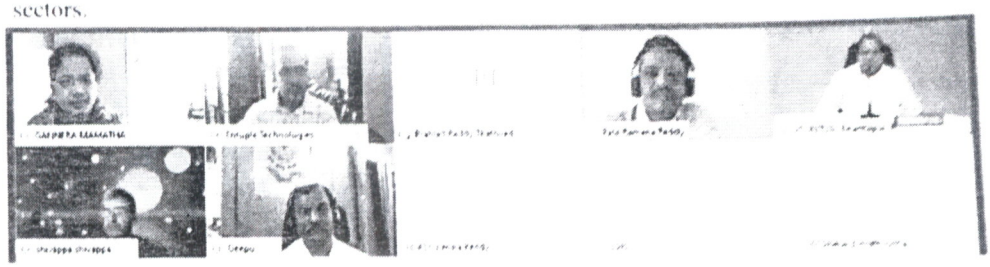
J.N.T.U. Anantapur
ANANTAPURAMU-515002

Department of Electronics & Communication Engineering
JNTUA College of Engineering (Autonomous), Ananthapuramu
Five-Day online Training Program on "ASIC Front End Design & Verification"
21 to 25 of September, 2020
Sponsored by TEQIP-III

REPORT

The department of Electronics and Communication Engineering has successfully organized a five-day workshop on the subject "ASIC Front End Design & Verification" in association with Entuple Technologies, Bangalore. The main objective of this 5 day program is to provide exposure to the participants on digital design and verification aspects of ASIC. The term ASIC stands for Application Specific Integrated Circuit. It is an integrated circuit customized for a particular use, rather than intended for general purpose use. This designing supports the development of embedded systems. In the recent years, there has been a significant increase in the demand for chip driven products especially for ASIC's in consumer electronics, medical electronics, communication, aero-space, computers and many other sectors.



On 21stthof September, the event began with the inaugural function at 9:30AM with University Invocation song. Prof S Srinivas Kumar has acted as chief guest and presented his views on the importance of VLSI, LOW Power VLSI and Image Processing for the students career point of view. He has invited industries to collaborate with the University for Knowledge gaining for both faculty and students and also encouraged multi disciplinary course incorporation in the University for the Students Benefit. Prof. K. Govidarajulu principal of the college, Prof. P. Ramana Reddy, Head of the Department, Mr. Damodaram M.S. Business Head, Entuple Technologies Pvt. Ltd., coordinators Prof. V. Sumalatha and Dr. G. Mamatha were present at the event.

Workshop – Day 1

Forenoon:

The morning session was taken over by Mr. K M Shivappa, who is the industrial expert at VLSI design. He is a 22 year experienced, very high-profile- senior design engineer at Entuple Technologies, Bangalore. It started with a power point presentation on their work at Entuple Technologies and their leading presence in Design and Verification using Verilog. It was continued with the explanation of Overview of VLSI, ASIC flow, FPGA flow, Industry Perspective

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Afternoon:

The Cadence tool – Incisive Enterprise Simulator is briefed in detail by the resource person and hands on designing of the basic AND gate as an design is explained to the students using a online meeting application Cisco-Webexby Mr. M S Damodara who has 19 years of industry experience

Workshop – Day 2 Forenoon:

The second day was initiated by Mr.M S Damodara who has 19 years of industry experience started with the basics of Digital Electronics like Number system , Logic gates , Realization of gates, Combinational Circuits and their application problems also basics of Verilog Language how to write and compile the Design written in Verilog language explained with a Power point presentation to the students using a online meeting application Cisco-Webex

Afternoon:

The afternoon session initiated by Mr.Naveen Sankar who has 8 years of industry experience started with designing of a simple Logic circuit using basic gates as instances for the design. This was took upto explain the Design by Writing a Verilog language for that instance and a basic thing that need to be kept in mind while writing the verilog code for the Design. Also guided in how to write a Test bench code for the Design to verify according to our specifications required.

The final written verilog code in Cadence – IES (Incisive Enterprise Simulator) was simulated and checked for any errors in the code. Upon successful simulation the variables are added to the Simvision which shows the output waveform for a simulated Design Code. Also explained with two more examples to students so that they can have a clear perspective of the Design and verifying the code.

Workshop –Day 3

Forenoon:

The third day started with Mr. AvinashKeshav , application engineer with 7 years of experience in VLSI industry demonstrated about Sequential Circuits , how they are designed and their mode of operation and their role in Designing Circuits .Explained about flipflops, counters ,registers and their necessity in the Design perspective through online meeting application Cisco-Webex.

Afternoon:

The afternoon session started with the designing of sequential Circuits their Design modeling and Simulation using Verilog language . Explained through an example like flipflops ,designed its code and written a testbench code for it to verify according to our specifications simulated the design and added the design variables to the Simvision to observe the output waveform in Cadence IES. Also explained sequential Modeling and simulation by considering two more examples

Workshop Day 4

Forenoon

The fourth day started with Mr. Vamshidhar Rao, application engineer with 7 years of experience in VLSI industry demonstrated about the design of State Machine and the procedure of various applications of the Design. Explained about Moore and Mealy State Machines by considering one example also explained the transition of bits in the another state depending on two types of sequences like Overlapped sequence and Non-Overlapped sequence and the is differences. Also explained the difference between Moore Mealy state Machine. Explained about Memories like RAM and ROM and their classification based on storage capacity and also about SRAM and DRAM and their circuit specifications and also their mode of operations and also about the Functional Verification.

Afternoon

The session was executed by Mr. M. S. Damodara who has 10 years of Industry experience demonstrated about AMBA APB Protocol the significance in designing a hardware and its operation. APB protocol is a Advance Peripheral Bus protocol which is used for both transfer of address data control signals to the peripherals connected and its operations how the data transfer occurs handshaking process reading the data writing the data and control signals and their transactions in a Bus architecture.

Workshop Day 5

Forenoon

The session was started with the APB protocol review a small recap by Mr. Avinash Kumar, application engineer with 7 years of experience in VLSI Industry. Explained APB protocol Verification how it does in an effective manner. And then started an another important topic Low Power Design Techniques. Now a days as the technologies is advancing effectively there must be a low power consumption and less leakage power in an Design with this advanced technology in VLSI Industry every Design must have a less power consumption and also it is a tradeoff between speed and time and explained a these techniques very effectively.

Afternoon

The session was held by Mr. M S Damodara, also shared their knowledge on power reduction techniques smoothly and also clarified the doubts of every student very peacefully and clearly. Also an request on students executed two more verilog design codes with a neat picture of design. Explained the State Machine case study by considering an example of Non-Overlapping and Non-Overlapping Sequences. At last there was a feedback from the students as a positive response regarding the 5 days online training program and how it helped them in this pandemic situation and had gained the knowledge how the VLSI Industry is emerging towards the new accomplishments made by an Engineer.

Online training program was ended with the token of gratitude note by Prof. V. Sumalatha and Dr. G. Mamatha to Mr. M S Damodara, and also entire Employee team who has been here all the whole monitoring students and making sure that they had gained knowledge on VLSI Industry Perspective.

TEQIP III

Certificate of participation

ENTUPLE

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) ANANTHAPURAMU

5 DAY ONLINE TRAINING PROGRAM ON

ASIC Front End Design & Verification

SPONSERED BY **TEQIP III**

This is to certify that Dr./Mr./Ms **Mamatha** has participated in 5 day online training program on

"ASIC Front End Design & Verification" during 21st to 25th September 2020

CO-ORDINATOR	CO-ORDINATOR	CONVENER	PATRON
Dr. G Mamatha	**Prof. V Sumalatha**	**Prof. P Ramana Reddy**	**Prof. K Govinda Rajulu**
Asst. Professor, ECE	Professor, ECE	Head, Department of ECE	Principal
JNTUA CEA	JNTUA CEA	JNTUA CEA	JNTUA CEA

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