TEQIP - III

C.B. NO. 150/2019-20 Head of Account TEQIP-III

Date: 06/09/19 Voucher No. 150/2019-20

Date: 06/09/19

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
COLLEGE OF ENGINEERING, ANANTHAPURAMU-515002

FULL VOUCHERED CONTINGENT BILL

Procs. No & date: TEQIP-III/NPIU/Academics/1-3-2(i)/18/2019-20 Dt: 11-7-2019

Purpose: Conducting three day workshop on in ECE Dept from 25th - 27th of July 2019

Payable to: Dr. G. Manmatha, Asst prof, Dept of ECE

Major Head: TEQIP-III Minor Head: 1-3-2(i)

No. of Sub Vouchers	Particulars	Amount Payable
	payable to Dr. G. Manmatha	51,382/-

Passed for Rs. 51,382/- (Rupees Fifty one thousand three hundred and eighty two rupees only)

Nodal Officer
Finance

Coordinator

Principal

Amount drawn under endorsed/your goodselves/ Vr No 150/2019-20 dated 06/09/19 for Rs 51,382/-

Date: 06/09/19

Principal

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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INDUSTRY APPLICATION SOCIETY STUDENT BRANCH CHAPTER

Three day Workshop On

Design and Layout Consideration of Mixed Signal IC

25th - 27th July 2019

In association with

ams Semiconductors India Pvt.Ltd&WnP technologies ,Hyderabad

Sponsored by **TEQIP III**

ATTENDANCE SHEET

26/07/2019 (AN)

SL.NO	ROLL NUMBER	NAME	SIGNATURE
1	18001D4301	S.SADIQ VALI	S.Sadiqvali
2	18001D4302	G .DEEPA	G.Deepa
3	18001D4303	P.SUJATHA	P.Sujatha
4	18001D4304	G.JAYAKRISHNA	G. Jayakrishna.
5	18001D4305	D.SATHEESH	D. Satheesh
6	18001D4306	G.CHITRAPRABHA	G.chitraprabha.
7	18001D4307	K LAVANYA	K.Lavanya
8	18001D4308	B LAVAKUMAR	B.L
9	18001D4310	S K AMEENA FIRDOWSE	Sk. Ameenfirdos
10	18001D4311	G KAVERI	G. Kaveri
11	18001D4312	N.PROMODA	N. Pramoda
12	18001D4313	Y.LATHA	Y. Latha
13	18001D4314	V AKHILA	V. Akhila
14	18001D4315	S MANJUSHA	S. Manjusha
15	18001D4316	P V TEJA JAYAKUMAR	
16	18001D4317	G HIMASAILA	G.Hima Saila.
17	18001D4318	C.KEERTHIKANTH	CKeerthikanth
18	18001D4321	K VIJAYAKUMAR	K.Vijaykumar
19	18001D4322	B.VIJAYANARASIMHAREDDY	Vijaya
20	18001D4323	P.V.N S SUMANTHRAJU	
21	18001D4324	S BALA KUMAR	S Balakumar
22	18001D4325	S.HARSHA VARDHAN REDDY	S.Harsha
23	18001D4326	S PRIYANKA	S.priyanka
24	18001D4327	J. DEEPTHY	Deepthi
25	18001D4319	M VISWANATH NAIK	M. Viswanath

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J.N.T.U. Anantapur
ANANTAPURAMU-515002

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

&

INDUSTRY APPLICATION SOCIETY STUDENT BRANCH CHAPTER

27th July 2019 AN

Three day Workshop On

Design and Layout Consideration of Mixed Signal IC

25th – 27th July 2019

In association with

ams Semiconductors India Pvt.Ltd&WnP technologies ,Hyderabad

Sponsored by **TEQIP III**

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10	18001D4311	G KAVERI	G.Kaveri
11	18001D4312	N.PROMODA	N. Promoda
12	18001D4313	Y.LATHA	Y. Latha
13	18001D4314	V AKHILA	V. Akhila
14	18001D4315	S MANJUSHA	
15	18001D4316	P V TEJA JAYAKUMAR	P.V.T.J
16	18001D4317	G HIMASAILA	G. Himasaila
17	18001D4318	C.KEERTHIKANTH	C.Keerthikanth
18	18001D4321	K VIJAYAKUMAR	K.vmi
19	18001D4322	B.VIJAYANARASIMHAREDDY	B.Vijaya Narasimha Reddy
20	18001D4323	P.V.N S SUMANTHRAJU	P.V.N.S.Sumanthraju
21	18001D4324	S BALA KUMAR	S.Bala Kumar
22	18001D4325	S.HARSHA VARDHAN REDDY	S.Harsha Vardhan Reddy
23	18001D4326	S PRIYANKA	S. Priyanka
24	18001D4327	J. DEEPTHY	J. Deepthi
25	18001D4319	M. VISWANATH NAIK	

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ANANTAPURAMU-515002

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Industry Application Student Branch Chapter

Organised

Three-day workshop on Design and Layout Considerations of Mixed Signal IC

25th to 27th July, 2019

in association with ams Semiconductors India PVT Ltd. and WnP Technologies, Hyderabad.

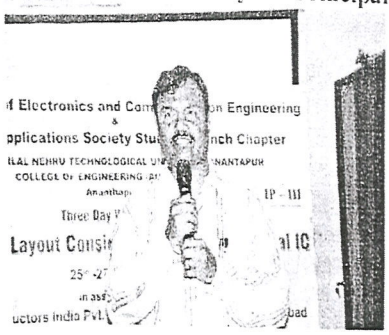
REPORT

The department of Electronics and Communication Engineering has successfully organized a three-day workshop on "Design and Layout Considerations of Mixed Signal IC" in association with ams Semiconductors India PVT Ltd. and WnP Technologies, Hyderabad. The objective of this workshop is to equip the students of M.Tech (VLSI) in the first year, second semester, hands-on with the knowledge of designing of mixed signal circuitry using the very versatile and in-demand Cadence design tool.

On 25th of July, the event began with the inaugural function at 9:30AM with prayer song and the lighting of lamp by the Principal of the college, Prof.Govindarajulu, the head of the department, Prof. P.Ramana Reddy, prof. Dr.V. Sumalatha and Mr. V. VeereshBabu, Senior Design Engineer, ams Semiconductors PVT Ltd, Hyderabad, Dr. G. Mamatha, who is the initiative behind this workshop gave the welcome note to the event. It was then followed by the address note by revered principal who through his presidential address, motivated the students for the best utilization of the resources and emphasized on the importance of opportunities with the present day industry demand. It was took forward by a short and encouraging address by the HOD. The industrial expert Mr. Veereesh, briefed on the subject of the workshop and its demand for mixed signal engineers. The inaugural function ended with a vote of thanks by Dr. G. Mamatha.

Lighting of the Lamp

Inaugural address by the Principal



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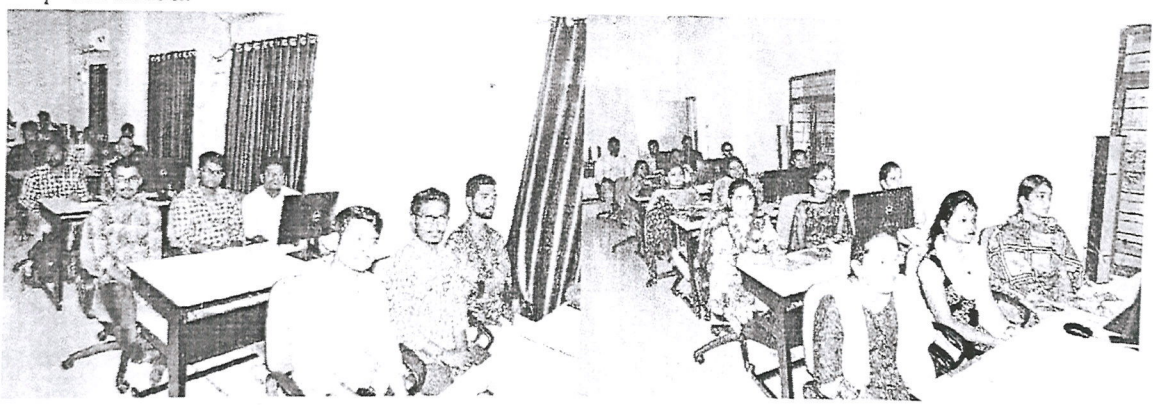
Workshop – Day 1

Forenoon:

Morning session was taken over by Dr. Veershbabu, who is the industrial expert at mixed signal design. He has 17 years experience in analog and mixed signal IC design, he is high-profile- senior design engineer at ams Semiconductors India Pvt. Ltd., Hyderabad.

Proceedings:
It started with a power point presentation on their work at ams and their leading presence in sensor based applications in the various domains. It was continued next with the explanation of analog, digital and mixed signal flow process flow and battery management system application system is taken as an example to showcase how a mixed signal design is implemented.



Afternoon:

The Cadence tool - Virtuoso is briefed in detail by the resource person and hands-on designing of the basic inverter as an amplifier design is explained to the students using a projector system.

Workshop - Day 2

Forenoon:

This design further revealed measuring of various components of small and large-signal analysis with the help of the tool and through the simulation and measurement, analysing

the behaviour of this signal with various the influence of various dependent parameters is illustrated.

Afternoon:

The afternoon session started with designing of a simple oscillator circuit using basic inverters as instances for the design. This was took up further on controlling of the frequency by varying values of currents and capacitor values. The further improvement of Oscillator circuit is the Voltage controlled oscillator. The design of this circuit is implemented as an extension of the previous.

The final schematic design of the day was designing PFD- Phase Frequency detector circuit. It need the designing of D- flipflop, which could later be integrated in PFD design.

Workshop -Day 3

The guest of the third day was Mr. SS Sharma Chinta, who is the Managing Director of WnP Technologies, Hyderabad. He has vast experience in the layout designing of the vlsi circuits. He is a thorough professional, with an experience of 29 years in the VLSI industry holding various post and profiles. He was introduced by the event initiative and organizer, Dr. G. Mamatha

PROCEEDINGS OF THE PRINCIPAL, JNTUA COLLEGE OF ENGINEERING ANANTHAPURAMU (AUTONOMOUS):: JNTUACEA ANANTHAPURAMU
PRESENT: Prof. K. RAMA NAIDU: PRINCIPAL

TEQIP-III

Procs. No. TEQIP-III/NPIU/Academics/1.3-2(i)/18/2019-20 Date:11-07-2019.

Sub: JNTUA College of Engineering Ananthapuramu - TEQIP-III - Academics – Permission to conduct three day workshop on "Design and Layout considerations of Mixed Signal IC" from 25-27, July 2019 at JNTUACEA-Orders-Issued.

Ref: Letter dt:09-07- 2019, from Dr. G. Mamatha, Asst. Professor, Dept. of ECE, JNTUACEA.

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Dr. G. Mamatha, Asst. Professor of ECE , JNTUACEA submitted a letter requesting the Principal to conduct three day workshop on "Design and Layout considerations of Mixed Signal IC" in association with ams Semiconductors India Pvt. Ltd and WnP Technologies, Hyderabad from 25-27, July 2019 at JNTUACE Ananthapuramu. The estimated expenditure for the same will be about Rs. 65,000/- and requested to meet the expenditure from TEQIP-III funds.

Title of the Programme	:	3- day workshop on "Design and Layout considerations of Mixed Signal IC"
Conducted by	:	Department of ECE, JNTUACEA
Dates of Workshop	:	25-27, July 2019
Coordinator	:	Dr. G. Mamatha, Asst. Professor of ECE, JNTUACEA

The requisition submitted is approved and the Principal is pleased to accord permission to Dr. G. Mamatha, Asst. Professor of ECE to conduct the above said programme on the date(s) noted. The expenditure will be met from TEQIP-III funds under Academics SC 1.3-2(i) head of account. The approximate expenditure for conduction of programme is Rs. 65,000/-.

It is requested to follow the rules and regulations in incurring the expenditure and requested to submit the vouchers in original as per the guidelines provided by NPIU. And also requested to submit Photographs, list of participants, feedback reports etc., as per TEQIP-III norms in Performa provided.

PRINCIPAL

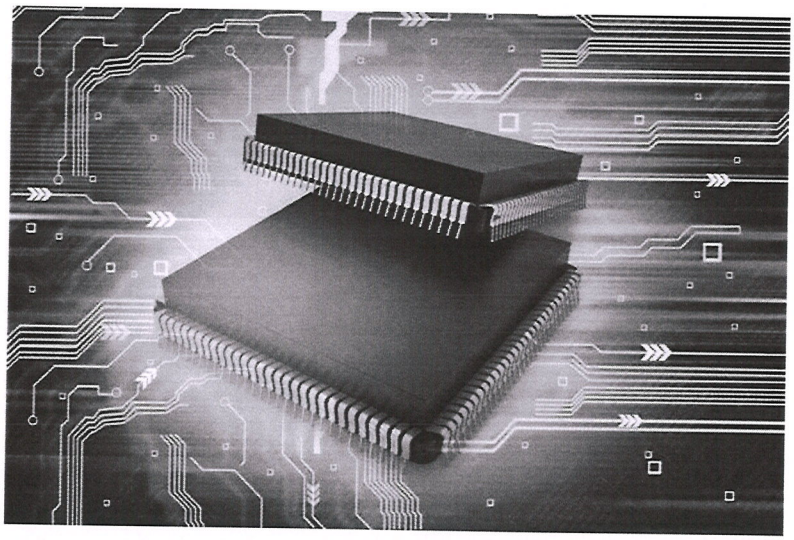
PRINCIPAL
J.N.T.U A College of Engg
(Autonomous)
ANANTHAPURAMU-5
A.P. INDIA.

To
Copy to Dr. G. Mamatha, Asst. Professor of ECE
Copy to HECED
Copy to Dr.A.P. Siva Kumar, TEQIP-III Co-ordinator & Nodal Officer (P)
Copy to Prof. E. Keshava Reddy, Nodal Officer (A) (TEQIP-III)
Copy to Dr.K. Jithendra Gowd, Nodal Officer (F) & TEQIP MIS officer
Copy to Bills.

Department of Electronics & Communication Engineering

JNTUA College of Engineering (Autonomous), Ananthapuramu

3- day WORKSHOP on " Design and Layout Considerations of Mixed Signal IC "



Date: 25th to 27th july 2019

RESOURCE PERSONS

DR. V Veeresh Babu
Senior Design Engineer ams
Semiconductor Hyderabad

Mr . SS Sharma Chinta
Managing Director of WnP

CONVENER
Prof. T . Sumalatha Head, Department of ECE
JNTUA CEA

CO-ORDINATOR
Dr. G Mamatha Asst. Professor, Department of ECEJNTUA CEA

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