Department of Electronics & Communication Engineering
JNTUA College of Engineering (Autonomous), Ananthapuramu

5 - Day Online Training Program on "ASIC Front End Design & Verification"
Sponsored by TEQIP-III

Date : 21st to 25th September 2020
Registration Link : https://rb.gy/nmm89z

About the College
JNTUA College of Engineering (Autonomous) Ananthapuramu, an esteemed engineering college in Andhra Pradesh was established in 1946 and has been growing continuously in size with respect to intake, faculty strength, number of academic programs offered and infrastructure. It is always committed to offer value added instruction to widen the horizon of vision for the enrichment of Technical education along with skill development.

About the Department
The department of Electronics and Communication Engineering is established in the year 1974. The department has come a long way since its inception, keeping pace with the changing needs and expectations of the society. At present, the department is running a full time UG program in Electronics and Communication Engineering, three PG programs in Digital Electronics & Communication Systems (DECS), VLSI System Design and Internet of Things specializations. The department conducts workshops, symposia, student and faculty development programs regularly on latest developments in the area of electronics and communication.

About Collaborating Partner - Entuple Technologies
Entuple is a next generation solutions enabler in cutting edge technologies. Entuple delivers world class simulation solutions in Applied Electromagnetics, Semiconductor (VLSI), System Design & Reliability, Mechanical, CFD and RF. Entuple has developed its own range of semiconductor based power drives and process control solutions. They cater to wide range of customers in semiconductor, manufacturing, defense & aerospace and academia.

Objective of the Program

VLSI technology has gone through rapid strides in last few decades. Designing efficient systems continuous to get more and more complex due to ever increasing demand for power, area and cost-effective solutions in digital and analog IC design. Understanding the importance, this online training program is aimed and designed keeping in mind the need of UG/PG Students as well as PhD Scholars and faculty members who are working in this area. This training program shall cover both theoretical as well as the demo sessions which will give good exposure to the participants on front end design and verification of digital systems. Various applications/case studies would also be covered.

Eligibility

Faculty/Research Scholars/UG & PG Students of ECE and allied branches are Eligible to apply.

Program Schedule

Date	Morning Sessions	Afternoon Sessions
21st Sep	Overview of VLSI, ASIC, FPGA flow – Industry Perspective	Getting started with Digital Design: Modeling & Simulation – DEMO
22nd Sep	Digital Design Stages, Modeling using Verilog	Design of Combinational Logic circuits using Verilog
23rd Sep	Modeling of Sequential Logic Circuits – Guidelines	Sequential Logic Circuits Modeling and Simulation – DEMO
24th Sep	Design of State Machines, Memories & Functional Verification	Protocol Verification: AMBA APB Protocol – Project Case Study Discussion
25th Sep	Protocol Verification: AMBA APB Protocol, Low Power Design Techniques	Design of State Machines – Project Case Study Discussion

CONVENER

Prof. P Ramana Reddy
Head, Department of ECE
JNTUA CEA

CO-PATRON

Prof. P Sujatha
Vice-Principal
JNTUA CEA

PATRON

Prof. K Govinda Rajulu
Principal
JNTUA CEA

CO-ORDINATORS

Dr. V. Sumalatha
Professor, Department of ECE
JNTUA CEA

Dr. G Mamatha
Asst. Professor, Department of ECE
JNTUA CEA

There is NO Registration Fee &
Last Date to Resister - 19th September 2020

Contact details for any Queries:
gmamatha.ece@jntua.ac.in
Ph: +91 9490446399
srinivas.b@entuple.com
Ph: +91 9908966658

RESOURCE PERSONS

1. Damodara M S, Business Head with 19 years of Industry experience
2. Shivappa K M, Director with 22 years of Industry experience
3. Navin Sankar, Sr. Design Engineer with 8 years of experience in VLSI domain
4. Avinash Keshav, Sr. Application Engineer with 7 years of experience in VLSI industry

INSTRUCTIONS TO PARTICIPANTS

- Link for the online Platform will be sent to the Registered Candidates Email ID.
- Attendance of 100% is compulsory for E-certification.