JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

COLLEGE OF ENGINEERING (Autonomous), PULIVENDULA

Y.S.R (KADAPA). Dist. A.P, INDIA 516 390

INVITATION TO TENDER AND

INSTRUCTIONS TO TENDERERS

FOR

PROCUREMENT OF EQUIPMENT

JNTUA COLLEGE OF ENGINEERING, PULIVENDULA

INVITATION TO TENDER AND INSTRUCTIONS TO TENDERERS

For the supply of Internet of Things Equipment, Mixed Signal Design Lab Software & Desktop Computers, UPS SMF Batteries and Desktop Computers for ELCS lab

JNTUA College of Engineering, Pulivendula invites tender for the supply of Internet of Things (IoT), Mixed Signal Design Lab Software & Desktop Computers, UPS SMF Batteries and Desktop Computers for ELCS lab to JNTUA College of Engineering, Pulivendula, as per specifications given in the schedule attached to the Tender form annexed hereto. All offers should be made in English and should be written in both figures and words.

The tender document can be obtained from the Principal, JNTUA College of Engineering, Pulivendula on payment of **Rs. 2,360/- (Rs. 2,000/- + 18% GST)** in the form of crossed Demand Draft on any Nationalised Bank drawn in favour of the "Principal, JNTUA College of Engineering, Pulivendula" payable at Pulivendula not earlier than **05.02.2019**. Alternatively the tender schedules can be downloaded from the website **www.jntua.ac.in or www.jntuacep.ac.in**. Such vendors who use downloaded tender schedules for submitting bids must enclose a demand draft for Rs. 2,000/- +GST 18% towards the tender fee along with the bid in addition to EMD for each tender schedule, otherwise the bid will be rejected.

Tender fee once paid is neither refundable nor adjustable for other tenders.

The JNTUA College of Engineering, Pulivendula reserves the right to select the item or to reject it. The JNTUA College of Engineering, Pulivendula also reserves the right to revise or alter the specifications of the Lab Equipments before acceptance of any tender.

The vendor has to submit the tender **separately for each schedule items** of the equipment. Incomplete tenders, amendments and additions to tender after opening or late tenders are liable to be ignored, and rejected.

EMD:

A Demand Draft, for an amount @2% of the estimated value of the schedule(s) for which the tenderer is submitting the bid, drawn in favour of the "Principal, JNTUA College of Engineering, Pulivendula" towards EMD must accompany the tender. Those without EMD will be rejected. The EMD will be refunded to all the unsuccessful tenderers only after the purchase orders are placed on the successful tenderer. The successful tenderer has to deposit an additional amount of 3% on the contract value as security money deposit.

The final acceptance of the material will be made only after delivering at our end in good condition and subject to satisfying all the specifications given by the University/College.

BID PRICE:

1. The contract shall be for the full quantity as described in the tender. Corrections, if any, shall be made by crossing out, initialling, dating and re-writing.

2. All duties, taxes and other levies payable by the vendor shall be included in the total price. Further, it is to be noted that JNTUA is registered with the Department of Scientific & Industrial Research (DSIR) for availing Customs/Central Excise duty exemption and the prices shall be quoted accordingly.

3. The rates quoted by the bidder shall be fixed for the duration of the contract and shall be included in the total price.

4. The prices should be quoted in Indian Rupees only.

5. The prices should be quoted with FOR destination.

6. Packing, forwarding, insurance etc. to vendors account.

7. After satisfactory installation, testing and demonstration, training has to be provided to faculty and staff to the satisfaction of the purchaser at vendor's cost.

8. The operation and maintenance manuals and lab manuals are to be supplied at vender's cost.

9. All essential accessories cost must be included in the price quoted.

10. The costs of essential spares are to be quoted separately. This will be taken into consideration while bids are evaluated.

11. Price bids are to be essentially signed by the vendor or person authorized by him.

12. Each bidder shall submit only one quotation. Alternatives offer option, if any, must be quoted in separate tender schedule.

VALIDITY OF QUOTATION:

Quotation shall remain valid for a period of three months after the deadline date specified for submission. The vendor shall extend the validity if required.

BIDDER QUALIFICATIONS:

1. The bidder must be ISO 9001-2008 certified company
2. Bidder must be a registered company with Goods and Service Tax, Sales Tax and Excise Departments and a true copy of such registration documents (PAN, GST, VAT, Service Tax & TIN) should be submitted along with the bid.
3. The bidder should submit the financial turnover report for the last three years.
4. The bidder should submit the list of customers (Govt. Organizations/Universities) along with year of supply and details of equipment supplied.
5. The bidders should submit Satisfactory Performance Certificate from the customers of this equipment. The product approval certificate, if any, from reputed organizations may also be submitted.

6. Bidder debarred/blacklisted by any Central or State Govt. / Quasi-Govt. Departments or organizations as on bid calling date for non-satisfactory past performance, corrupt, fraudulent or any other unethical business practices shall not be eligible.
7. The Principal, JNTUA College of Engineering, Pulivendula reserves the right to assess the capacity/capability of the suppliers in the overall interest of the Institute without assigning any reason.

EVALUATION OF QUOTATIONS:

The purchaser will evaluate and compare the quotations determined to be substantially responsive i.e whether they are:

a) Are properly signed; and

b) Conform to the terms and conditions, and specifications mentioned in this

c) The quotations unless otherwise specified would be evaluated separately for each item, and

d) If the bidder is not the Original Equipment Manufacturer (OEM) they must provide an authorization certificate from the Original Equipment Manufacturer, stating that the bidder is an approved agent of OEM and service warranty will be guaranteed by OEM in case the agent's license is aborted or any other reason whatsoever during the warranty period.

AWARD OF CONTRACT:

The purchaser will award the contract to the bidder whose quotation has been determined to be substantially responsive and who has offered the lowest evaluated quotation price.

1. Notwithstanding the above, the purchaser reserves the right to accept or reject any quotations and to cancel the bidding process and reject all quotations at any time prior to the award of contract.
2. The institution reserves the right to place the orders for individual items with different tenders.

3. **Right to Acceptance:**

   The Principal, JNTUA College of Engineering, Pulivendula does not bind himself to accept the lowest on any tender and reserve to himself the right of accepting the whole or any part of the tender or portion of the quantity offered the tenderer shall supply the same at the rate quoted.
4. The bidder, whose bid is accepted, will be notified for the award of contract by the purchaser prior to expiry of the quotation validity period. The terms of the accepted offer shall be incorporated in the purchase order.

DELIVERY:

All the goods ordered shall be delivered with proper packing within 15 days from the date of issue of order.

TERMS OF PAYMENT:

a) **Payment shall be made by JNTUA College of Engineering, Pulivendula**, after delivery at the specified location, and after installation, commissioning and satisfactory demonstration of the goods with all specifications and standards to the entire satisfaction of the college.
b) The bidder may give the details of bank Account into which the payments are to be made.
c) Normal commercial warranty/guarantee shall be applicable to the supplied goods.

DELIVERY OF TENDER:'

Bid for schedule of the tender is to be placed in a bigger envelope, clearly mentioning schedule No._____on it. The Envelop must be super-scribed with the reference No. (JNTUACEP/LAB EQUIPMENT/TENDERS/S.No_____/2019, dated:05.02.2019).

The sealed tender should be addressed to:

The Principal,
JNTUA College of Engineering,
Muddanur Road, Pulivendula – 516390
Y.S.R. (Dist.), A.P., India.

Bids in sealed covers should reach the above address latest by 16.00 hours on 26-02-2019. Tenders submitted after the specified time shall not be considered and no intimation will be sent in this regard.

The college reserves the Right to reject any tender which fails to comply with the above instructions. All tenders should be sent by Post or through messenger, to drop the tender in the sealed tender box provided in the office. It is the responsibility of the tenderer to see that his tender offer is delivered by the specified time at the above address. All further communication should be addressed to the officer named above and by title only.

OTHER TERMS:

Tenderer should make their representative available on **26-02-2019 at 16.00 hrs** at the time of opening tenders in the chambers of Principal or any other designated place within the college.

The tenderer should produce Goods and Services Tax (GST) & Value Added Tax (VAT) - Registration certificate.

Tenderer should responsible and bear any price escalation within the validity period and also after the indent has been placed till the supply.

Sd/-PRINCIPAL

SUMMARY OF TENDER SCHEDULES

TENDER REFERENCE	:	JNTUACEP/LABEQUIPMENT/ Dept ..... Sch.No---/2019, dated:05.02.2019).
DATE OF COMMENCEMENT OF SALE OF BIDDING DOCUMENT	:	DATE 05.02.2019 TIME: 10:00 Hrs
LAST DATE FOR SALE OF BIDDING DOCUMENT	:	DATE 26.02.2019 TIME: 15:00 Hrs
LAST DATE AND TIME FOR RECEIPT OF BIDS	:	DATE 26.02.2019 TIME 16:00 Hrs
TIME AND DATE OF OPENING OF BIDS	:	DATE 26.02.2019 TIME 16:30 Hrs
PLACE OF OPENING OF BIDS	:	JNTU College of Engineering, Muddanur Road, Pulivendula – 516 390 Kadapa District Andhra Pradesh
ADDRESS FOR COMMUNICATION	:	**The Principal, JNTU College of Engineering, Muddanur Road, Pulivendula – 516 390, Y.S.R (District), Andhra Pradesh**

BID PARTICULARS

1. Name of the Supplier :

2. Address of the Supplier :

3. Address of the Show Room/Workshop :

4. Display of goods : Yes / No

5. EMD enclosed : Yes / No

DD No. _____ Bank: _____ Amount: _____

6. Name and address of the officer to whom all reference shall be made regarding this tender enquiry

Name :

Address :

Telephone No.:

Fax No. :

Mobile No. :

e-mail :

Website :

FORMAT OF QUOTATION

S. No	Schedule No... (As given in the Annexure)	Description of Goods	Specifications	Qty	Unit	Quoted Unit rate in Rs.	Total Amount	
							In Figures	In Words

Gross Total Cost: Rs. _____

We agree to supply the above goods in accordance with the technical specifications for a total contract price of Rs. _____ (Amount in figures) _____ (Rs. Amount in words) within the period specified in the invitation for Quotations.

We also confirm that the normal commercial warrantee / guarantee of _____ months shall apply to the offered goods.

Signature of Supplier
with seal

ABSTRACT OF EQUIPMENT

Dept.	Schedule No	Name of the Equipment/ Lab	Quantity	Estimated Amount (in Rs.)
ECE	S.1	**Mixed signal Design Lab Software**		
		Xilinx Vivado Software	25 users	154770.00
		Mentor Graphics Front End Tools	25 Users	367500.00
		Mentor Graphics Back End Tools	25 Users	367500.00
			Total	**8, 89,770.00**
ECE	S.2	**Desktop Computers for Mixed signal Design Lab**		
		Desktop Computers	15 no.	**960000.00**
CSE	S.3	**Internet of Things Equipment**		
		IoT Development Boards	01	289108.00
		Add on Shields	01	29560.00
		Wireless Modules	01	96370.00
		Sensors	01	129962.00
		Prototyping and Consumables	01	172070.00
			Total	**7, 17,070.00**
CSE	S.4	**SMF Batteries for UPS**		
		SMF Batteries	128 No.	**5,07,520.00**
H&S Dept.	S.5	**Desktop Computers for ELCS lab**		
		Desktop Computers	65 No.	**32,50,000.00**

Sd/-
PRINCIPAL

SCHEDULE –S.1

Mixed signal Design Lab Software

Schedule No	Name of the Equipment	Quantity	Estimated Amount	EMD Amount
S.1	Xilinx Vivado Software	25 users	154770.00	17795.00
	Mentor Graphics Front End Tools	25 Users	367500.00	
	Mentor Graphics Back End Tools	25 Users	367500.00	
		Total	**8, 89,770.00**	

Detailed specifications of Schedule are given below.

Component Model	Latest Version of each software given above
Warranty	2 Years
Installation	On-site with free of cost
On-site Support	Servicing, Technical Support and training of the staff for a period of 2 years

Note : All the items in the list has to be supplied by single vendor.

XilinX Vivado Design Suite- System Edition – 25 Users: - Latest Edition Software

- The Vivado® Design Suite should delivers a SoC-strength, IP-centric and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation.
- The Vivado Design suite should be generation ahead in overall productivity, ease-of-use, and system level integration capabilities.
- Vivado should supports the following device families: Ultrascale, Virtex-7, Kintex-7, Artix-7, and Zynq -7000 .The Vivado® Design Suite should comprises of following modules for Design and Integration of Software-defined IP Generation with Vivado High-Level Synthesis, Model-based DSP Design Integration with System Generator for DSP, Block-based IP Integration with Vivado IP Integrator
- Vivado High Level Synthesis – should be Fast time to QoR that rivals hand-coded RTL driven architecture-aware synthesis that delivers the best possible QoR Vivado Logic Simulation should be Integrated Mixed Language Simulator,Integrated & Standalone Programming and Debug Environments to Accelerate Verification with C, C++ or System C with Vivado HLS
- Implementation of 4X Faster Implementation for Better Design Density & Up to 3-Speedgrade Performance Advantage for the low-end & mid-range.

- The SDSoC™ development environment should provide a familiar embedded C/C++ application development experience including an easy to use Eclipse IDE and a comprehensive design environment for heterogeneous Zynq® All Programmable SoC and MPSoC deployment.
- Complete with the industry's first C/C++ full-system optimizing compiler, SDSoC delivers system level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming. It also enables end user and third party platform developers to rapidly define, integrate, and verify system level solutions and enable their end customers with a customized programming environment.
- Easy to use Eclipse IDE to develop a full Zynq All Programmable SoC and MPSoC system with embedded C/C++ applications
- Accelerate a function in Programmable Logic (PL).

Technical Specifications For Mentor Graphics Front-End IC Design Tools Package – 25 Users : - Latest Edition Software

- The Mentor Graphics Front-End IC Design Tools Package should consist of following modules and should meet the requirements mentioned below.
    1) Requirement Tracing Module.
    2) Design Entry Module.
    3) Functional Verification Module.
    4) Formal Verification Module.
    5) FPGA Synthesis Module.
    6) ASIC Synthesis Module.
    7) DFT Module.
    8) Logic Equivalence Checking Module.

1. <u>Requirement Tracing Module.</u>

a. The software should trace requirements through hardware design process by linking requirements from different sources.

b. The software should support addition of following documents to the project
    i. User Requirements,
    ii. Acceptance Tests,
    iii. Design Specification,
    iv. RTL Design Files (VHDL, Verilog, System Verilog),
    v. Testbench Code (VHDL, Verilog, System Verilog and PSL),

vi. Verification Results,
vii. Post-Synthesis and Post PnR Results.

c. The software should support tracing of all the requirements through the design process, implementation process and the verification process with either top-down or bottom-up approach.
d. The software should support generation of various types of reports like traceability matrices, impact analysis, inconsistent requirements, and customized reports.
e. The software should be able to generate reports output in a wide variety of formats – Microsoft Office, Adobe PDF, HTML.
f. The software should have an in-built reviewer feature to enable the user to validate the requirements.
g. The software should be able to integrate with FPGA and ASIC design tools.
h. The software should be supported on Windows and Linux Platform.

2. <u>Design Entry Module.</u>

a. The software should have the following design entry capabilities:--
   i. Block Diagram
   ii. Interface-Based Design (IBD)
   iii. State Diagram (FSM).
   iv. Algorithmic State Machine (ASM).
   v. Flow Chart
   vi. Truth Table
   vii. Built-In text Editor (DesignPad)
   viii. Library of common functions
b. The software should have Full support for following languages:--
   i. Verilog 1995/2001/2005.
   ii. VHDL 1987/2002/2008.
   iii. SystemVerilog 1800.
c. The software should have integration with digital Simulation Tool for Remote Simulation control and cross probing.
d. The software should be capable of performing Design Integrity Check.
e. The software should support code to graphics conversion (Block Diagram, IBD, Flow Chart and FSM views) for the imported RTL codes.
f. The software should support Documentation at all design phases in html format.
g. The software should have integration with Requirements Tracing Tool

h. The software should support RTL rule checking to analyze the quality of the HDL code.
i. The software should have following in-built Rule Libraries for Design Checking (Linting):--
    i. DO-254.
    ii. RMM.
    iii. Xilinx Specific.
    iv. Altera Specific.
    v. Essential Rules.
    vi. Safety Critical Rules.
j. The software should allow users to customize the available rules.
k. The software should have Design Management features for both ASIC and FPGA(all vendors):
    i. Provides a centralized database for the complete design data- RTL as well as non-RTL.
    ii. Version control on all the design data.
l. The software should have integration with the Synthesis and PAR tool for any FPGA family.
m. The software should be supported on Windows and Linux Platform.

3. <u>Functional Verification Module.</u>

a. The software should support the following languages:--
    i. Verilog 1995/2001/2005.
    ii. VHDL 1987/1993/2002/2008.
    iii. System Verilog IEEE 1800 Design.
    iv. System Verilog IEEE 1800 Verification
    v. System Verilog Assertion
    vi. PSL IEEE 1850.
    vii. Verilog PLI/VPI.
    viii. System Verilog DPI.
    ix. VHDL FLI.
    x. System C 2.2 IEEE 1666/OSCI 2.2
b. The software should support mixed-language simulation.
c. The software should support SDF Files for Timing Simulation.
d. The software should support Assertion Based Verification.
e. The software should support Constraint-Random Test Generation.

f. The software should have Verification Methodology Support (OVM and UVM).
g. The software should support Functional Coverage.
h. The product should provide Industry-leading RTL and gate-level simulation performance using the advanced global simulation optimization feature having advanced features like Pre-Optimized Design Unit and compile SDF feature.
i. The software should support following Code Coverage Matrices:--
    i. Statement Coverage.
    ii. Branch Coverage.
    iii. Condition & Expression Coverage. (FEC & UDP).
    iv. FSM Coverage. (State, Transition & Sequence Coverage)
    v. Toggle Coverage.
    vi. Extended Toggle Coverage.
j. The software should allow debugging Delta Delay Issues using Wave Window and List Window.
k. The software should have VCD to WLF Conversion Utility.
l. The software should be supported on Windows & Linux Platform.

4. <u>Formal Verification Module.</u>

a. The software should be able to achieve coverage closure.
b. The software should be able to do clock domain crossing verification.
c. The software should be able to perform formal analysis directly on the RTL.
d. The software should be able to address issues such as connectivity, X-states, reset structures and design constraints.
e. The software should be able to do property checking to address issues of I/F protocols, functional coverage, control logic, data integrity and post-silicon debug.
f. The software should able to work directly on RTL to automatically synthesize assertions and perform formal sequential analysis without testbench or user-written assertions.
g. The software should be supported on Linux Platform.

5. <u>FPGA Synthesis Module.</u>

a. The software should support following CPLD/FPGA Vendors:--
    i. Xilinx.
    ii. Altera.
    iii. Actel.
    iv. Atmel.
    v. Lattice.
    vi. QuickLogic.

b. The software should support Pre-PnR Physical synthesis across multiple vendors to reach design goals faster, in less iteration.
c. The software should support Automatic Incremental Synthesis to minimize the impact of late cycle design changes in addition to partition based Incremental Synthesis.
d. The software should support Resource Manager to make efficient use of FPGA architectural blocks with cross-probing into RTL as well as Technology schematics.
e. The software should support synthesis of VHDL, Verilog, System Verilog and Mixed HDL Designs.
f. The software should support integration with ESL, Equivalence Checking, PCB and Requirements Tracing Tools.
g. The software should be supported on Windows & Linux Platform.

6. **ASIC Synthesis Module.**
   a. The software should support ASIC synthesis.
   b. The software should have an in-built capability to convert generic libraries (.lib) into tool specific libraries.
   c. The software should support Verilog, VHDL and Mixed Language Design Synthesis.
   d. The software should provide highest QoR with the speed and features needed for large designs.
   e. The software should have true hierarchical support for Incremental Synthesis.
   f. The software should support different design flows like flat or hierarchical, top-down, or bottom-up.
   g. The software should have in-built graphical viewer with powerful debugging and analysis capabilities.
   h. The software should be supported on Windows and Linux Platform.

7. DFT Module.
   a. Scan Insertion Software.
      i. The software should support scan insertion on Verilog Gate Level Netlist.
      ii. The software should support following three types of scan cells for the purpose of scan insertion.
         1. Mux-DFF.
         2. Clocked Scan.
         3. LSSD.

iii. The software should support identification and insertion of full scan, partial scan, wrapper chains and test points.
iv. The software should provide powerful scannability checking/reporting capabilities for sequential elements in the design.
v. The software should perform design rules checking to ensure scan setup and operation is correct, before scan is actually inserted.
vi. The software should insert IEEE 1500 compliant test structures to enable block-based testing strategies for SoC designs.
vii. The software should support wrapper scan insertion for Hierarchical Designs.
viii. The software should provide integrated graphical viewer for schematic graphical debugging.
ix. The software should support Graybox Functionality.
x. The software should be able to work in all design environments using any combination of synthesis, place-and-route, and verification tools.
xi. The software should have an in-built shell that enables the users to manipulate and query the design data. It should support the following features:--
    1. Design Editing.
    2. Hierarchical Design Introspection.
    3. Setting and Reading Attributes.
xii. The software should be supported on Linux Platform.

b. <u>Compression & ATPG Software</u>
i. The software should support ATPG on scan-inserted Verilog Netlist.
ii. The software should produce an efficient, compact pattern set.
iii. The software should support following fault models:--
    1. Stuck-at.
    2. IDDQ.
    3. Transition.
    4. Path Delay.
    5. Static Bridge.
    6. Timing Aware (small delay defect).
    7. Cell-Aware.
    8. Multiple Detect.
    9. User-Defined Fault Model (UDFM).

iv. The software should support ATPG for all scan styles, multiple scan chains, multiple scan clocks, plus gated clocks, set and reset lines.

v. The software should provide easy and flexible scan setup using a test procedure file.

vi. The software should provide DFT rules checking (before pattern generation) to ensure proper scan insertion.

vii. The software should provide pattern compression capabilities to ensure small, yet efficient test patterns.

viii. The software should support generating following types of patterns :--

1. Basic Scan Patterns.
2. Clock PO Patterns.
3. Clock Sequential Patterns.
4. Multiple Load Patterns.
5. RAM Sequential Patterns.
6. Sequential Transparent Patterns.

ix. The software should provide support for timing exception path constraints in SDC format.

x. The software should support reading Verilog Netlist and generating EDT Logic as per the user's specifications.

xi. The software should use embedded deterministic test technology to achieve the highest level of test quality while reducing test time and test data volume.

xii. The software should provide flexible design flow that supports any synthesis tool or strategy.

xiii. The software should support use of on-chip PLL for at-speed testing.

xiv. The software should ensure shorter time to market with integration into all design flows and foundry support.

xv. The software should provide at-speed solution that includes transition, multiple detect transition, timing-aware, and critical path testing.

xvi. The software should support integration with simulator for automated simulation mismatch analysis.

xvii. The software should provide Test Coverage, Fault Coverage and ATPG Effectiveness.

xviii. The software should support Graybox Functionality.

xix. The software should have an in-built shell that enables the users to manipulate and query the design data. It should support the following features:--

1. Design Editing.
2. Hierarchical Design Introspection.
3. Setting and Reading Attributes.

xx. The software should support different test pattern formats:--

1. ASCII
2. Binary
3. Wave Generation Language (WGL)
4. Standard Test Interface Language (STIL)
5. Verilog
6. ASIC Vendor Data Formats like TI TDL 91, Fujitsu FTDL-E, Mitsubishi TDL, Toshiba TSTL2.

xxi. The software should be supported on Linux Platform.

c. Memory BIST Software.

i. The software should support generation and insertion of memory BIST into RTL or gate-level netlist.

ii. The software should provide a complete solution for at-speed Memory Testing and Diagnosis.

iii. The software should support hierarchical based approach allowing BIST to be added to individual cores as well as the top level.

iv. The software should support insertion of configurable Memory BIST Controllers to support a variety of memory types, as well as range of memory timing interfaces and memory port configurations.

v. The software should support insertion of controllers that can be accessed and controlled through the test access port (TAP) interface using IEEE 1149.1 and IEEE 1500 protocols or through a specified CPU Interface.

vi. The software should support insertion of controllers that can be accessed throughout the life of the integrated circuit, including manufacturing test, silicon debug and system verification.

vii. The software should support comprehensive automation flow that provides design rule checking, test planning, integration and verification all at the RTL or Gate Level.

viii. The software should support hard-coding of one or more in-built or user programmed memory test algorithms into the controllers.

ix. The software should support the capability to select shorter test algorithms for optimizing test time.

x. The software should have a large library of common memory test algorithms.

xi. The software should support all leading memory IP like TSMC, Virage, ARM, Dolphin, MoSys.

xii. The software should support unlimited number of memories, ports and configurations per Memory BIST Controller.

xiii. The software should support memories with built-in test interfaces.

xiv. The software should support comprehensive set of field proven memory test algorithms.

xv. The software should support the following Diagnostic Capabilities:--

1. Direct Compare Approach.
2. Stop-On_Error Approach.

xvi. The software should support at-speed diagnostics.

xvii. The software should provide a high level code of commonly used algorithms for direct use or as a reference for a user modified algorithm. The available algorithms should include March X, March Y, March C-, March LA, Row Bar, Column Bar, Masest, GalPat, GalRow, GalCol, WalkingPat, 1x1 Checkerboard, 4x4 Checkerboard, Bit Surround Disturb.

xviii. The software should support Automated Memory Test Resource Optimization wherein the controllers are automatically configured and assigned to memories based on several criteria/constraints like clock domain, test time, power dissipation and physical layout (lef/def).

xix. The software should support verification of inserted Memory BIST Logic both at the core level and top level.

xx. The software should be supported on Linux Platform.

d. <u>Boundary Scan Software.</u>

i. The software should provide solution for the creation and integration of boundary scan cells and related control logic for embedded test and diagnosis of integrated circuit I/Os, as well as test and diagnosis of board-level interconnects between ICs.

ii. The software should provide a completely automated solution for adding standard boundary scan support to ICs of any size or complexity, reducing IC engineering development effort and improving time-to-market

iii. The software should supports standard 1149.1 boundary scan cells, 1149.1 custom boundary scan cells, and optionally 1149.6 boundary scan cells for dif-ferential I/O cells driving AC-coupled nets.

iv. The software should be supported on Linux Platform.

8. <u>Logic Equivalence Checking Module.</u>

a. The software should support Verilog, VHDL, System Verilog and Mixed Language both at the RTL Level and Gate-Level.

b. The software should support supports both ASIC and FPGA Design Flows.

c. The software should provide support for probing from objects to design schematic.

d. The software should have an integrated schematic viewer to trace and view paths.

e. The software should be able to correlate design errors to root causes.

f. The software should have capability to help narrow down errors.

g. The software should analyze individual targets and identifies error.

h. The software should have an integrated Debug Schematic that graphically displays targets showing error sources and also supports cross reference to RTL or netlist source.

i. The software should be able to accept inputs from any synthesis tool.

j. The software should support RTL to RTL, RTL to GATE, and GATE to GATE Level Verification at all the design stages.

k. The software should have an in-built analyzer that reports the potential error sites and the logic values.

l. The software should have an in-built formal analysis capability that detects and reports design conditions that have the potential to cause unintended circuit behavior.

m. The software should have support for full-cross highlighting between RTL model and circuit.

n. The software should support pruned schematics that shows only the logic that directly contribute to the error or its propagation and hence reduces the debugging effort.

o. The software should have support for User Constraints File.

p. The software should provide the flexibility to generate the reports at every tool step with an option of summarized report or detailed reports.

q. The software should be supported on Windows & Linux Platform.

Technical Specifications For Mentor Graphics Back-End IC Design Tools Package – 25 Users : - Latest Edition Software

- The Mentor Graphics-Back-End IC Design Tools Package should consist of following modules and should meet the requirements mentioned below.
    1) Schematic Entry Module.
    2) Analog/RF Simulation Module.
    3) Mixed-Signal Simulation Module .
    4) Layout Module.
    5) Physical Verification Module.
    6) Parasitic Extraction Module.
    7) 3D EM Design & Verification Module.

1. <u>Schematic Entry Module.</u>

a. The software should support a simulation cockpit for fast setup of simulations of AMS and RF circuits under a variety of conditions.
b. The software should have easy simulation setup for complex mixed-signal designs.
c. The software should have Models blocks using schematic representations, VHDL, Verilog, SPICE, or VHDL-AMS, and enables simulation of the entire design.
d. The software should offer advanced schematic data modeling techniques, as well as an integrated simulation cockpit and revision control system
e. The software should allow user to capture schematic designs.
f. The software should provide predefined hotkeys and supports user-defined hotkeys.
g. The software should support stroke and function key shortcuts.
h. The software should allow user to specify hierarchical designs using top-down and bottom-up methods.
i. The software should have predefined component libraries.
j. The software should allow editing in the context of a design viewpoint allowing different design processes to occur simultaneously.
k. The software should support custom userware developed with AMPLE
l. The software should be supported on Linux platform.

2. <u>Analog / RF Simulation Module.</u>

a. The software should have Core Technology allowing addressing Analog Circuit Simulation.
b. The software should Support simulation of very large circuits (up to around 300,000 transistors) in time and frequency domain.

c. The software should support 3X to 10X gain in simulation speed over the other commercial SPICE simulators, while maintaining the accuracy.
d. The software should support transient simulation algorithms OSR, Newton and IEM.
e. The software should have Flexible user control of simulation accuracy.
f. The software should have transient noise algorithm.
g. The software should support circuit simulation on different levels of abstraction (transistor level, gate level, structural, behavioral).
h. The software should have In built Optimizer.
i. The software should support Advanced analysis options such as pole-zero, enhanced Monte-Carlo analysis, Sensitivity, Worst Case, DC, AC, Transient.
j. The software should support S and Z-domain generalized transfer functions.
k. The software should support Reliability simulation.
l. The software should Support Verilog-A Language.
m. The software should have extensive model libraries including leading MOS, Bipolar and MESFET transistor models such as BSIM3V3.x, BSIM 4, MM9, Mextram and HICUM.
n. The software should Support IBIS model.
o. The software should have graphical post-processor which provides all graphical basic functions such as zoom, data measurement, curve tracing and parametric plotting.
p. The software should extract characteristics of Power consumption, 3dB frequency, settling time and propagation delay.
q. The software should support Full-chip RF IC verification.
r. The software should provide a set of dedicated algorithms to accurately and efficiently handle the multi-GHz signals in modern wireless communication applications.
s. The software should have Should have Multi-tone, steady-state analysis for large RF IC designs containing thousands of elements
t. The software should be supported on Linux Platform.

3. <u>Mixed-Signal Simulation Module.</u>

a. The software should support Mixed Signal simulation environment with flexible abstraction support through the standard mixed-signal languages (Verilog-AMS and VHDL-AMS) and/or SPICE-level models and support for multiple simulation modes (SPICE, analog, mixed-signal and digital).

b. The software should support single executable language-based mixed signal simulation.
c. The software should support support standard analysis like DC, AC, Transient, Noise, Transfer function, Sensitivity, Transient noise & Native reliability analysis and measurement scripting language.
d. The software should support Monte Carlo and parametric statistical analysis, sweeping analysis and circuit parameters analysis capabilities.
e. The software should enable parasitic stitching and reduction for post-layout design and verification.
f. The software should have Digital and real number-modeling capabilities.
g. The software should be supported on Linux platform.

4. <u>Layout Module.</u>

a. The software should provide connectivity and constraint driven layout environment to support the physical implementation of analog, custom digital and mixed signal designs at device, cell block and chip level.
b. The software should support common constraint environment as used in Schematic Editor.
c. The software should have the ability to automate custom design.
d. The software should have the ability to include standard cells to automate editing for example abutment, pin permutation, folding, chaining, cloning, synchronous cloning etc.
e. The software should support graphical cell view option in layout editor.
f. The software should have the ability for interactive editing in layout design such as design rule check violation visualization detection and correction.
g. The software should support Schematic and/or SPICE netlist driven layout and flow.
h. The software should support On-the-fly DRC while performing standard editing commands.
i. The software should have Ready-to-use parameterized device generators for digital and analog layout design.
j. The software should have Integrated Engineering Change Order (ECO) component.
k. The software should support High-capacity database editing.
l. The software should have LEF/DEF interface.
m. The software should be supported on Linux Platform.

5. Physical Verification Module.

a. Design Rule Checking (DRC) Software.

i. The software should support DRC on the following layers: Original Layers, Derived Polygon Layer's, Derived Edge Layers and Derived Error Layers.

ii. The software should support Edge-based rule checking: Identification of geometry widths & lengths is made simple.

iii. The software should support early write of nmDRC errors: Need not wait for all checks to be completed for debugging errors.

iv. The software should support rectangular based operation.

v. The software should support Rule-based verification: enables comprehensive failure analysis in a single robust environment.

vi. The software should support All-angle checking: Allows verification of complex analog components.

vii. The software should support grouping of checks.

viii. The software should support conditional checks.

ix. The software should support Select/Unselect checks before DRC run.

x. The software should support Select/Unselect checks by layer before DRC run.

xi. The software should support DRC HTML reporting of side RDBs (Result Database).

xii. The software should have Layout Window / Windel: Allows specification of coordinates of layout for verification.

xiii. The software should detect even the most complex Antennas in the design.

xiv. The software should support for Planarity & Density check.

xv. The software should limit number of discrepancies in the report.

xvi. The software should support DRC run in command mode.

xvii. The software should support Dual Database Capability.

xviii. The software should highlight Errors in different context.

xix. The software should support Boolean operation which is faster than polygon topological operation.

xx. The software should support flat DRC.

xxi. The software should support Identification of Net Area Ratio Errors.

xxii. The software should support direct access to OpenAccess database.

xxiii. The software should support Running Layout vs. Layout check.

xxiv. The software should support access to databases -- GDSII, OASIS, LEF/DEF.

xxv. The software should support Mapping the schematic and layout hierarchy despite layout cells are having different names.

xxvi. The software should support for Hierarchical DRC comparison.

xxvii. The software should support Incremental Verification: allows debugging within a seconds rather than hours.

xxviii. The software should support Concurrent checking capability: Allows simultaneous running of multiple check.

xxix. The software should support rectangular based operation.

xxx. The software should have Ability to exclude cells during verification.

xxxi. The software should show hierarchical result counts first.

xxxii. The software should support Multi-Threading.

xxxiii. The software should support Distributed Computing.

xxxiv. The software should support Hyperscaling: allows parallel processing of layout operation.

xxxv. The software should support Boolean operation which is faster than polygon topological operation.

xxxvi. The software should be supported on Linux Platform.

b. <u>Layout VS Schematic (LVS) Software.</u>

i. The software should support for Flat LVS comparison.

ii. The software should support LVS run in command mode.

iii. The software should Compare various types of design types: GDS2-to-netlist, Netlist-to-netlist

iv. The software should have Built-in detection of following devices: CMOS N Transistor, CMOS P Transistor, NMOS Enhancement Transistor, NMOS Depletion Transistor, MOS Generic Transistor, CMOS LDD N Transistor, CMOS LDD P Transistor, NMOS LDD Enhancement Transistor, NMOS LDD Depletion Transistor, MOS LDD Generic Transistor, Resistor, Capacitor, Diode, Bipolar Transistor, JFET Transistor, Inductor, and Voltage Source.

v. The software should support extraction of Flat Layout Netlist.

vi. The software should have ASCII database for connectivity extraction using SVDB.

vii. The software should generate the errors in the form of report and GUI.

viii. The software should generate the Layout netlist and source netlist after the connectivity extraction.
ix. The software should support identification of misspelled text in layout or source.
x. The software should support Identification of Non functional text.
xi. The software should support Identification of the hard connection errors in the rule file.
xii. The software should support Identification of soft connection errors using STAMP statement.
xiii. The software should support Identification of soft connections using SCONNECT statement.
xiv. The software should support virtually connect unconnected nets.
xv. The software should support Easy identification of opens.
xvi. The software should support Easy identification of Shorts.
xvii. The software should support Easy identification of power to ground short.
xviii. The software should support Identification of Malformed devices.
xix. The software should support for tracing properties (i.e Ambiguity Resolutions) values.
xx. The software should support Command line invocation of LVS.
xxi. The software should Allow device instances having arbitrary device names to serve as built-in device instances for LVS comparison.
xxii. The software should support following gate recognition features: Recognize all gates, Recognize simple gates.
xxiii. The software should support Short Isolation, which isolates the short by finding the shortest path between 2 or more pieces of conflicting text.
xxiv. The software should allow floating pins in sub circuit calls in SPICE netlists during LVS comparison.
xxv. The software should stop all LVS comparisons if a problem is encountered with either the power or ground.
xxvi. The software should support for Hierarchical LVS comparison.
xxvii. The software should support for Hcell file during the cell name mismatch in the source and layout.
xxviii. The software should support hierarchical LVS comparison.
xxix. The software should support Distributed Computing.
xxx. The software should support Hcell Analysis on placement.

xxxi. The software should support Hyperscaling: allows parallel processing of layout operation.

xxxii. The software should support Automation in generation of HCELL files.

xxxiii. The software should be supported on Linux Platform.

c. Result Viewing Environment & Interactive GUI Software.

i. The software should have easy integration with most layout environments.

ii. The software should have a fast debugging time for cell, block and full-chip designs.

iii. The software should provide fast, flexible and easy-to-use graphical debugging capabilities that minimize the turnaround time and tapeout-clean on schedule.

iv. The software should support QDB-H: command mode of accessing the LVS hierarchical database.

v. The software should support print internal schematic in LVS compare.

vi. The software should support the following features when used in conjunction with DRC:

1. Intuitive GUI to simplify debugging.
2. Sort DRC results by cell or by checks.
3. Mark results as fixed after correcting the error in the layout.
4. Mark results as waived for subsequent DRC runs.
5. Highlights DRC results in context in which they occur.

vii. The software should support the following features when used in conjunction with LVS:

1. Highlight LVS results in layout & schematic, source & extracted netlists.
2. Fast and intuitive SPICE browser to highlight devices from the netlist windows.
3. Query any net in the Layout.
4. Use device highlight filters to control which device types to highlight.
5. Query any Instances in the layout.
6. Use Include & Exclude window filters to control area of highlighted net in layout.
7. Cross-Highlight between schematics, design layout and the LVS result report.

viii. The software should support the following features when used in conjunction with Parasitic Extraction :
    1. Uses Parasitic Browsing window to easily & quickly see extracted values of parasitic in a simple window.
    2. Sort parasitic results by name or by value to quickly find nets of interest or with large parasitic values.
    3. Search specific nets by name.
    4. Highlights C, R and CC results into layout and schematic windows.
    5. Accurate timing and performance simulations for leading-edge circuit designs.
    6. Enables quick and easy navigation of extraction results and perform both interactive and batch point-to-point calculations.
ix. The software should have Intuitive graphical interface.
x. The software should have Built-in memory for common run-tasks with runset support.
xi. The software should have Customized runset options.
xii. The software should support Triggers (Internal and External).
xiii. The software should be supported on Linux Platform.

6. **Parasitic Extraction Module.**
    a. RC Extraction Software
        i. The software should support various netlist formats: Hspice, Spectre, DSPF, SPEF.
        ii. The software should include various parasitic models: C-only netlist, R-only netlist, RC netlist, RCC netlist.
        iii. The software should support tight integration with nmLVS: provides complete circuit Netlist information integrated to the source schematic for back-annotation.
        iv. The software should have robust parasitic extraction tool that delivers accurate parasitic data for comprehensive and accurate post-layout analysis and simulation.
        v. The software should be able to extract interconnect parasitic hierarchically.
        vi. The software should support various levels of extraction: Transistor Level Extraction, Gate Level Extraction, Hierarchical Level Extraction, Selected Net Exclusion, and Selected Net Extraction.
        vii. The software should run in command line mode or batch mode.

viii. The software should be able to exclude specific nets from extraction.
ix. The software should be able to limit extraction to specific nets.
x. The software should support comparison of total coupling capacitance between any two net pairs in the extracted results to a user specified threshold.
xi. The software should perform parasitic element reduction of distributed RC extraction data.
xii. The software should support TICER – RC reduction for netlist size reduction in Distributed RC Netlist.
xiii. The software should perform parasitic element reduction of both distributed RC and Lumped C.
xiv. The software should generate report for distributed RC parasitic results of the extracted circuit.
xv. The software should generate report for lumped C parasitic results of the extracted circuit.
xvi. The software should specify thresholds for distributed RC parasitic extraction.
xvii. The software should support New Resistor End points.
xviii. The software should support Maximum width and spacing of Capacitor.
xix. The software should support extraction of Floating Nets in the design.
xx. The software should support Multi-Corner extraction in single run.
xxi. The software should support advanced Manufacturing effects include CMP aware extraction.
xxii. The software should support various layout file formats: GDS II, LEF/DEF, OASIS.
xxiii. The software should support mixed mode extraction
xxiv. The software should support noise, timing, power and SI analysis.
xxv. The software should be supported on Linux Platform.

b. <u>Inductance Extraction Software.</u>
i. The software should support various netlist formats Formats: Hspice, Spectre, DSPF, SPEF.
ii. The software should include parasitic models: L and L+M along with C-only netlist, R-only netlist, RC netlist, RCC netlist. Remarks: Distributed Resistance and Capacitance, Lumped Capacitance, Self and Mutual impedance.

iii. The software should model Skin and Proximity Effects.
iv. The software should have Broadband Netlist Generation.
v. The software should extract Self and mutual impedance.
vi. The software should be able to limit extraction to specific nets.
vii. The software should support various layout file formats: GDS II, LEF/DEF, OASIS.
viii. The software should be supported on Linux Platform.

7. **3D EM Design & Verification Module.**
    a. The software should accurately model complex structures on packages, PCBs and IC/MMIC circuits for optimized system performance.
    b. The software should support Automatic 3D geometry model creation with features for modeling entire interconnect paths on package and board, including bond wires, solder balls & bumps, vias, and routing traces.
    c. The software should support the distributed computing technology, which simulates the full structure with the optimal solution in a reasonable length of time.
    d. The software should deliver multiport S-parameter models (Touchstone Format) and broadband RCLK Spice sub circuit models.
    e. The software should be capable of real-time parameter tuning and optimization.
    f. The software should support Antenna and RF/Microwave designs.
    g. The software should be able to perform enhancing Multi-gbps simulation.
    h. The software should support Automatic non-uniform mesh generation—even novice users with limited numerical modeling skills can easily achieve expert-level results.
    i. The software should have Intuitive graphical user interface provides a large set of polygon and vertex-based editing facilities, speeding up EM structure definition and parameterization.
    j. The software should support True 3D metallic structure modeling that places no limitation on shape or orientation; easily model conical vias, conical helix antennas, wire bonds and any planar microwave or RF structures.
    k. The software should be compatible with Hspice model simulation
    l. The software should be supported on Windows & Linux Platform.

Xilinx FPGA Evaluation Platform with interfacing cards- 2no.

- Entry-level FPGA board should be designed exclusively for the Vivado Design Suite, featuring Xilinx Artix 7-FPGA architecture. This includes the standard features found on all fpga boards: complete ready-to-use hardware, a large collection of on-board I/O

devices, all required FPGA support circuits. Features the Artix-7 FPGA : XC7A35T-1CPG236C

- 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops).
- 1,800 Kbits of fast block RAM
- Five clock management tiles, each with a phase-locked loop (PLL)
- 90 DSP slices
- Internal clock speeds exceeding 450MHz.
- On-chip analog-to-digital converter (XADC).
- This FPGA should be expansive line-up of ports and peripherals to introduce system-level design concepts:
    - 16 user switches
    - 16 user LEDs.
    - 5 user pushbuttons.
    - 4-digit 7-segment display ,4 Pmod connectors, 3 Standard 12 pin Pmod, 1 dual purpose XADC signal/ standard Pmod ,12-bit VGA output.
    - USB-UART Bridge,Serial Flash,USB-JTAG port for FPGA programming and communication.
    - USB HID Host for mice, keyboards and memory sticks.
    - The PmodKYPD is a peripheral module featuring a 16-button keypad. The keys are numbered in a hexadecimal fashion (0-9, A-F). It uses a standard 12-pin Pmod header that will indicate which row and which column has been pressed in the array of buttons.

SCHEDULE –S.2

Desktop Computers for Mixed signal Design Lab

Schedule No	Name of the Equipment	Quantity	Estimated Amount	EMD Amount
S.2	Desktop Computers	15 No.	**9,60,000.00**	19,200.00

Detailed specifications of Schedule are given below.

Component Make	Specified by the Vendor
Component Model	Specified by the
Warranty	3 Years
Installation	On-site with free of cost
On-site Support	Servicing, Technical Support for a period of 3 years

Technical Specifications

S.No.	Item	Specifications
1	Make and Model	should be specified by the Vendor
2	Form Factor	Tower
3	Processor	Intel Core i5-8400 (6 Cores/9 MB/6T/up to 4.0 GHz/65 W) processor
4	Chipset	H 370 chipset or higher
5	Memory	8 GB DDR4- memory Up to 2 DIMM slots 2666 MHz DDR4 SDRAM, expandable up to32 GB
6	Storage	1TB 7200rpm SATA Hard Drive
7	storage features	System should support upto2 TB of SATA Harddisk and up to 512 GB of solid state drives
8	Optical Drive	DVDRW
9	Communications	Ethernet LAN 10/100/1000 controller
10	Graphic Card	AMD Radeon™ R5 430, 2GB Graphic card with display port
11	Monitor	19.5 inch Monitor
12	Operating Systems	Windows 10 Professional 64bit operating system
13	Power Supply	260Watts 80 PLUS EPA Bronze 85% effcient
14	Ports	8 External USB: 4 x USB 3.1 Gen 1 and 4 x USB 2.0 1 RJ-45; 1 Display Port ; 1 HDMI 1.4; 1 UAJ
15	Slots	1 full height PCIe x16, 3 full height PCIe x1, 2 M.2

16	Bays	4 Bays(1 internal 3.5” HDD, 2 internal 2.5” HDD, 1 external slim ODD)
17	Audio	Realtek AIC 3234 Audio Codec with internal speaker
18	Security	Trusted Platform Module2 TPM 1.2 or 2.0, chassis lock slot support chassis Intrusion switch, Setup/BIOS Password
19	Keyboard	USB Standard 104 Keys Key Board
20	Mouse	USB Optical Mouse
21	Warranty	3 years on site warranty

SCHEDULE –S.3
Internet of Things Equipment

Schedule No	Name of the Equipment	Quantity	Estimated Amount	EMD Amount
S.3	IoT Development Boards	01	289108.00	
	Add on Shields	01	29560.00	
	Wireless Modules	01	96370.00	
	Sensors	01	129962.00	
	Prototyping and Consumables	01	172070.00	
		Total	**7, 17,070.00**	

Detailed specifications of Schedule are given below.

Component Make	Specified by the Vendor
Component Model	Raspberry pi 3
Warranty	2 Years
Installation	On-site with free of cost

IoT Development Boards

Name of the component	Quantity
Raspberry Pi 3 (Made in UK), Single Board Computer	15
Arduino Uno R3 with USB Programming Cable	15
Node MCU - ESP8266 IoT Development Board	10
Beaglebone Black Rev C	5
Intel Edison with Arduino Breakout Board	2
Particle Photon (WiFi IoT Development Board)	5
Arduino Genuino 101 (Intel Curie Dev Board with onboard BLE)	5
LPG Gas Sensor (MQ2)	30
Body Temperature Sensor	20
Blood Pressure Sensor	6

Add on Shields for above Dev Boards

Name of the component	Quantity
LCD Shield	5
Sense Hat for Raspberry Pi	5
SD Card Shield	5
RTC Module shield	10
Dot Matrix display Module with MAX 7219 IC	5

Wireless Modules

Name of the component	Quantity
ESP-8266-01 - WiFi Module	10
Bluetooth Low Energy BLE HM-10	10
Bluetooth Classic Module HC-05	10
RFID Module With RFID Cards (3 tags)	10
GSM/GPRS Module (SIM 800)	10
GPS Module (Ublox 6M)	5
Finger Print Module (R305)	2
Raspberry Pi Camera Module (8Mp Camera V2)	10

Sensors

Name of the component	Quantity
HC SR-04 (Distance Sensor)	10
PIR Sensor (Motion Detection Sensor)	10
DHT 11 (Humidity and Temperature Sensor)	10
LM35 (Temperature Sensor)	10
LDR (Light Sensor for Arduino)	20
BH1750 Sensor (Light Sensor for Raspberry Pi 2)	5
Colour Sensor	5
Soil Moisture Sensor	10
ADXL sensor (Accelerometer Sensor) ADXL345	10
Water proof Temperature Sensor (DS18B20)	10
Xbee S2c series with Base board	10
Alcohal sensor Module (MQ-03)	10
Air quality sensor Module (MQ-135)	10
Carbon Monoxide Sensor Module (MQ-07)	10
Smoke Sensor (MQ-02)	10
Barometric Pressure Sensor (BMP 10)	10
Compass Module (HMC5885)	10
DHT22 Humidity and Temp sensor Module	10
Flex Sensor 2.2	5
Flex Sensor 4.2	5
Force sensor	5
IR Long Range sensor	5
IR Obstacle Avoidance sensor	10
Pulse Sensor	5
Raindrop sensor	10
Reflective Optical Sensor with Transistor Output	10
Sound Sensor Module	10
Tilt sensor Module	10
Hall effect sensor Module	10
ECG Module	2
EMG/EKG Shield	2

Prototyping and Consumables

Name of the component	Quantity
Breadboard (Medium size)	10
Breadboard (Normal size)	20
Dot Board (Small size)	10
Dot Board (Medium size)	10
Dot Board (Large size)	10
Power Adapters for Raspberry Pi 3	15
Power Adapters for Beaglebone Black	5
Power Adapters for GSM/GPRS Module	10
16gb Class 10 Sd Card for pi 3	15
HDMI to VGA Convertors	15
Ehternet Cables	15
LEDS	500
De-soldering Pump	5
Resistor Box	10
Capacitor Box	10
Laser Doide	10
Digital Multimeter	10
Multimeter Probes	10
Push Buttons	100
Potentiometer	50
Stepper Motors -5v	10
Stepper Motors -12v	10
stepper Motor Driver Module	20
Batteries (9V Hw)	10
Snap Connectors with Power Plug	10
Servo Motor-1kg torque	10
Servo Motor-5kg torque	10
USB to RS232 Convertor	10
1-channel relay module	10
4-channel relay module	5
Buzzer	20
Raspberry Pi cases	15
Aluminium heat sinks	15
LCD 16*2 character	15
32 in 1 screw tool kit	10
8gb sd card for raspberry	15
4-digit seven display	10
16keypad membrane	10
7-segment display	20
Assorted connecting wires (M-M) (M-F) (F-F)	1000
Soldering wire	2
Breadboarding wire	2
Solderon Iron	10
Soldering Stand	10
Soldering Lead 50Gm	10
Cutter	10
Stripper	10
32 in 1 Screwdriver tool kit	5
Glue Gun	5
Glue Stick	20

SCHEDULE –S.4

SMF Batteries for UPS

Schedule No	Name of the Equipment	Quantity	Estimated Amount	EMD Amount
S.4	SMF Batteries	128 no.	**5,07,520.00**	

Detailed specifications of Schedule are given below.

Battery Make	Standard make - Specified by the Vendor
Battery Model	Sealed Maintenance Free (SMF) Lead Acid
Nominal Voltage	12V
Battery Capacity	100 Ah
Battery Warranty	3 Years
Installation With sufficient iron racks	On-site with free of cost
Maintenance	**Annual maintenance for two years**

SCHEDULE –S.5
Desktop Computers for ELCS lab

Schedule No	Name of the Equipment	Quantity	Estimated Amount	EMD Amount
S.5	Desktop Computers	65 no.	**3250000.00**	

Detailed specifications of Schedule are given below.

Sl No	Description/Make & Model	Technical Specification
1	Make and Model	should be specified by the Vendor
2	Form Factor	Tower Model
3	Processor	Intel Core i5-8400 (6 Cores/9 MB/6T/up to 4.0 GHz/65 W) processor
4	Chipset	Intel B360 Chipset; OEM Motherboard with TPM 2.0
5	Memory	8GB-DDR4 RAM; Expandable Upto 32GB or higher; 2 DIMM Slots
6	HDD	1TB SATA 7200rpm HDD or higher
7	Audio	Integrated High Definition (HD) Audio with Internal Speaker built into CPU
8	Optical Drive	DVD Burner (DVD±RW)
9	Keyboard and Mouse	104 Keys keyboard and optical mouse
10	Ethernet	Integrated Gigabit Ethernet Connection
11	Ports	1. Front Pots: - 2*USB 3.1 Gen 2, 4*USB 3.1 Gen 1, microphone (3.5mm), headphone (3.5mm). 2. Rear Ports: - 2*USB 3.1 Gen1, 2*USB 2.0, 1*Serial, One Ethernet (RJ-45), 1*VGA, 1*Display Port, one HDMI Line-in (3.5mm), line-out (3.5mm), microphone (3.5mm).
12	Slots	2*PCI/PCIe Slots 2*M.2 Card Slots

13	Security Features	● Power-on password ● Administrator password ● Padlock loop ● Hard disk password ● Boot sequence control ● Boot without keyboard and mouse ● Individual USB port disablement
14	Power Supply	180 watts, autosensing, 85% PSU or higher
15	Monitor	19.5 inch
16	Operating System	Genuine Windows 10 Pro 64 Bit Preloaded
17	Warranty	3 Years Onsite Warranty
Optional:		
18	Headsets	1. Input Impedance: 32 Ohms. 2. Sensitivity (headphone): 100dB +/-3Db 3. Sensitivity (microphone): -58dBV/µBar, -38dBV/Pa +/-4dB. 4. Frequency response (Headset): 20Hz - 20 kHz. 5. Frequency response (Microphone): 100Hz - 16 kHz. 6. Cable length: 1.8m. 7. Rotating microphone feature