JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
ANANTAPURAMU-515 002 (A.P.), INDIA

COURSE STRUCTURE
AND
DETAILED SYLLABI
OF
MASTER OF TECHNOLOGY
IN

VLSI and Embedded Systems, Embedded Systems and VLSI, VLSI and Embedded Systems Design

For Regular Two Year P.G. Degree Course

(Applicable for the batches admitted from 2012-13)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

Revised Course Structure and Syllabi for

M.Tech-VLSI and Embedded Systems, Embedded Systems and VLSI and VLSI and Embedded Systems Design

Offered by Department of ECE

for Affiliated Engineering Colleges 2012-13

I YEAR I Semester

S. No	Course code	Subject	Theory	Lab.	Credits
1.	9D57101	VLSI Technology	4	0	4
2.	9D06102	Embedded System Concepts	4	0	4
3.	12D68101	Analog & Digital IC Design	4	0	4
4.	9D57104	Hardware Description Languages	4	0	4
5	9D06101	Digital System Design	4	0	4
6.	12D68102 12D68103 12D68104	Elective – I a. MEMS b. RF IC Design c. Device Modeling	4	0	4
7.	12D68105	Simulation and Synthesis Lab		3	2
		Contact periods/week	24	3	
		Total	27		26

I YEAR II Semester

S. No	Course code	Subject	Theory	Lab.	Credits
1.	9D55204	FPGA Architectures & Applications	4	0	4
2.	12D68201	Memory Technology	4	0	4
3.	9D55202	Real Time Operating Systems	4	0	4
4.	12D68202	DSP Architectures and Applications	4	0	4
5.	12D68203	ASIC Design	4	0	4
6.	12D68204 12D68205 12D68206	Elective – II a. Software Defined Radio b. VLSI Signal Processing c. Design & Testability	4	0	4
7.	12D68207	FPGA Design Lab		3	2
		Contact periods/week	24	3	
		Total	27		26

II YEAR (III & IV Semesters)

S. No	Course code	Subject		credits
1	12D68401	Seminar		2
2	12D68402	Project work		16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th 4** **C 4**

(9D57101) VLSI TECHNOLOGY

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

UNIT II

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT III

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

UNIT IV

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT V

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT VI

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VII

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT VIII

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th** **C**

4 **4**

(9D06102) EMBEDDED SYSTEM CONCEPTS

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

UNIT IV

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT V

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

UNIT VI

INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VII

SYSTEM DESIGN TECHNIQUES:

Design methodologies, requirement analysis, specifications, system analysis and architecture design

UNIT VIII

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes..

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D.Givargis, John Willey, 2002

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th** **C**

4 **4**

(12D68101) ANALOG & DIGITAL IC DESIGN

UNIT I

MOS transistors- modeling in linear, saturation and cutoff high frequency equivalent circuit.

UNIT II & III

INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT IV

OVER SAMPLING CONVERTERS AND FILTERS: Over Sampling With and Without Noise Shaping .Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

UNIT V

CMOS Inverter characteristics (static & dynamic in brief treatment), Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design.

UNIT VI&VII

LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT VIII

SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuit" Tata-Mc GrawHill, 2002
2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999

REFERENCES:

1. D.A.JOHN & KEN MARTIN: "Analog Integrated Circuit Design". John Wiley, 1997.
2. Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1997

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th** **C**

4 **4**

(9D57104) HARDWARE DESCRIPTION LANGUAGES

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT V

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT VI

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT VII

INTRODUCTION TO VHDL: An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

UNIT VIII

BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

TEXT BOOKS:

1. M.D.CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Z.NAWABI, "VHDL Analysis and Modeling of Digital Systems", (2/E), McGraw Hill, 1998.

REFERENCES:

1. M.G.ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.
2. PERRY, "VHDL", (3/E), McGraw Hill.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th 4** **C 4**

(9D06101) DIGITAL SYSTEM DESIGN

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT II

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT III

FAULT MODELING: Fault classes and models, Stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT IV

TEST PATTERN GENERATION: D–algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT V

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT VI

PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding.

UNIT VII

PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT VIII

ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. N. Biswas – "Logic Design Theory" (PHI)
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCES:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th** **C**

4 **4**

(12D68102) MEMS
ELECTIVE I

UNIT-I

INTRODUCTION: history of MEMS, market for MEMS, overview of MEMS processes properties of silicon, a sample MEMS process. Basics of Micro technology: definitions and terminology, a sample process, lithography and etching. MEMS Biosensors: Bio Flow Sensors, MEMS Images. Introduction to MEMS Pro design software.

UNIT-II

MICROMACHINING: subtractive processes (wet and dry etching), additive processes (evaporation, sputtering, epitaxial growth). Fundamental Devices and Processes: basic mechanics and electrostatics for MEMS, parallel plate actuators, pull-in point, comb drives.

UNIT-III

FUNDAMENTAL DEVICES AND PROCESSES: more electrostatic actuators; MEMS foundries, Cronos MUMPs (multi user MEMS process). MUMPs Multi User MEMS Process: JDS Uniphase MUMPs processing sequence and design rules.

UNIT-IV

MUMPs and **SUMMIT**: design rules; applications; micro hinges and deployment actuators.

UNIT-V

CMOS MEMS: CMOS foundry processes, integrated IC/MEMS, MEMS post processing, applications.

UNIT-VI

CLEAN ROOM LAB TECHNIQUES: clean rooms, gowning procedures; safety, fire, toxicity; acids and bases, photolithography.

UNIT-VII

MICROOPTOELECTROMECHANICAL SYSTEMS (MOEMS): micro scanners, digital mirror display, retinal scanning display. Grating light valve,

UNIT-VIII

Corner cube retroreflector, optical switches, other micro-optical devices.
applications.

TEXT BOOKS:

1. HSU, TAI RAN, MEMS and Microsystems Design and Manufacture, Tata Mc Graw-Hill,2002.
2. Rai-Choudhury, Prosenjit; Mems and Moems Technology and Applications SPIE 2000.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th 4** **C 4**

(12D68103) RF IC DESIGN
ELECTIVE I

UNIT I
BASIC CONCEPTS IN RF DESIGN: Nonlinearity and Time Variance, Inter symbol Interference, Random Processes and Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation

UNIT II
MODULATION AND DETECTION: General Considerations, Analog Modulation, Digital Modulation, Power Efficiency of Modulation Schemes, Noncoherent Detection

UNIT III
MULTIPLE ACCESS TECHNIQUES AND WIRELESS STANDARDS: Mobile RF Communications, Multiple Access Techniques, Wireless Standards

UNIT IV
TRANSCEIVER ARCHITECTURES: General Considerations, Receiver Architectures, Transmitter Architectures, Transceiver Performance tests, Case Studies

UNIT V
LOW-NOISE AMPLIFIERS AND MIXERS: Low-Noise Amplifiers, Down conversion mixers, Cascaded Stages Revisited.

UNIT VI
OSCILLATORS: General Considerations, Basic LC Oscillator Topologies, Voltage-controlled Oscillators, Phase Noise, Bipolar and CMOS LC Oscillators, Monolithic Inductors, Resonator-less VCOs, Quadrature Signal Generation, Single-sideband Generation

UNIT VII
FREQUENCY SYNTHESIZERS: General Considerations, Phase-Locked Loops, RF Synthesizer Architectures, Frequency Dividers.

UNIT VIII
POWER AMPLIFIERS: General Considerations, Classification of Power Amplifiers, High-Efficiency Power Amplifiers, Large-Signal Impedance Matching, Linearization Techniques, Design Examples.

TEXTBOOKS:

1. Behzad Razavi, "RF Micro Electronics", PHI publishers, 1998.
2. John Rogers, Calvin Plett, "Radio Frequency Integrated Circuit Design", Artech house Inc, London, 2003.
3. Chris Bowick, "RF Circuit Design", Newness, Elsevier Science, 1982.
4. Willuam F. Egan, "Practical RF System Design", John Wiley & Sons, Inc., 2003.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **Th 4** **C 4**

(12D68104) DEVICE MODELING
ELECTIVE I

UNIT I

OVERVIEW of MOS: Characteristics of a MOS transistor-Surface properties of Silicon : Energy band diagram for the ideal case-Calculation of the threshold voltage(vt) – Non ideal effects- CV plots: importance – Ideal case – High frequency CV plots – low Frequency CV plots – Equations to CV plots – Deep depletion – Deviations from the Ideal CV plots: interface traps, Effect of AC signal on the interface states.

UNIT II

Techniques to measure Cit, computation of Cs and Ps – Limitation in high frequency techniques – Comparison of measurements at high and low frequency techniques.

UNIT III

Sources of Oxide Trapped charge – radiation created oxide trapped charge – Experimental results – How Oxide Trapped charge can be annealed out – models to explain the technique – Shifts in threshold voltage in P-channel and N-channel MOSFET – Disadvantages – Shifts at dynamic bias – radiation hardening – Other alternatives dielectrics – gate metallization

UNIT IV

MOSFET- Parameters of importance – Qualitative analysis of MOSFET – Mathematical model of IV characteristics – SPICE level1, level 2, level 3 models – Change in velocity with electric field – Expression for Id in the sub threshold region of operation.

UNIT V

Non uniform doping and effect on threshold voltage – short channel effect – Narrow width effect – Small Geometry effects – Shrink and Scaling.

UNIT VI

Small signal analysis of MOSFET – Derivation of the different parameters associated with the small signal model – Cutoff frequency – Hot carrier effects – 1988 model – Monte-Carlo analysis

UNIT VII

MOSFET devices – HMOS, DMOS, DIMOS, UMOS, VMOS, Sy MOSFET, SOS, Si MOX, BESOI, SEU, FAMOS, MCOS – Comparison with the conventional CMOS.MOS

UNIT VIII

Device application: Depletion mode device – MOSFET connected as load devices - MOSFET as resistors, Static protection.

TEXT BOOK:

1. Dewitt G. Ong, "Modern MOS technology: processes, Devices and Design", McGraw-Hill, 1984.
2. Sorab K.Gandhi, "Semiconductor Device Principle", John Wiley & Sons, 1994.

REFERENCE BOOKS:

1. Sze S.M., "VLSI technology", McGraw-Hill, 2003.
2. P Antognetti, G Massobrio, *Semiconductor device modelling with SPICE*, McGraw-Hill

P Ashburn, *Design and realization of bipolar transistors*, Wiley 1988.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. I SEM (VLSI & ES) **L C**

3 2

(12D68105) SIMULATION AND SYNTHESIS LAB

1. Introduction to MATLAB Programming
2. Program assembly, Execution, Data processing and graphic analysis
3. Application of FFT for signal processing
4. Signal processing – Signal generation, filter design and analysis
5. MATLAB program to plot the one-dimensional rectangular potential well with infinite potential barrier
6. Numerical solution of the Schrodinger wave equation for rectangular potential well with infinite potential barrier using MATLAB program.
7. Design and simulation of (i) Combinational logic circuits, (ii) Sequential logic circuits, (iii) Analog circuits and (iv) A/D mixed circuits
8. Synthesis of Digital Circuit.
9. Place and Router Techniques for FPGAs.
10. Implementation of Design using FPGA and CPLD Devices.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th 4** **C 4**

(9D55204) FPGA Architecture & Applications

UNIT-I

Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD's–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures–3000 Series–Speed Performance and in system programmability.

UNIT-II

FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.

UNIT-III

Case Studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's–ACT-1, 2, 3 and their speed performance.

UNIT-IV

Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs, Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

UNIT-V

Finite State Machines (FSM)-II Alternative realization for state machine chart using microprogramming. Linked state machines, One–Hot state machine, Petrinetes for state machines–basic concepts, properties, Extended petrinetes for parallel controllers. Finite State Machine–Case Study, Meta Stability, Synchronization.

UNIT-VI

Fsm Architectures and Systems Level Design Architectures centered around non-registered PLDs, State machine designs centered around shift registers, One – Hot design method, Use of ASMs in One – Hot design. K Application of One – Hot method, System level design controller, data path and functional partition.

UNIT-VII

Digital front end Digital Design Tools for (FPGAs & ASICs) using Cadence EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs.

UNIT-VIII

Guidelines and Case Studies Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Text Books:

1. P.K.Chan & S. Mourad, "Digital Design using Field Programmable Gate Array," Prentice Hall, 1994.
2. S.Trimberger, Edr., "Field Programmable Gate Array Technology," Kluwer Academic Publications, 1994.
3. J. Old Field, R. Dorf, "Field Programmable Gate Arrays," John Wiley & Sons, Newyork, Reprint 2008.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array," Kluwer Publications, 1992, 2nd Edition.

Reference Books:

1. Richard F Jinder , "Engineering Digital Design," 2nd Edition, Academic press.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th 4** **C 4**

(12D68201) Memory Technology

UNIT – I

Introduction to Non-Volatile Memory: Introduction, Elementary memory concepts, Unique aspects of Non-volatile memory, Flash memory and flash cell variations, Semiconductor device Technology Generations.

UNIT – II

Flash Memory Applications: Spectrum of memory devices, Evolving from EPROMs, Evolution of Flash usage models, Understanding flash attributes, Code storage, Data storage, Code and Data storage.

UNIT – III

Memory Circuit Technologies: Flash cell basic operation, Flash memory architecture, Redundancy, Error correction coding, Design of testability, Flash Specific circuit techniques.

UNIT – IV

NOR Flash stacked and Split-Gate Memory Technology: ETOX Flash cell Technology, SST Super-flash EEPROM cell technology, Reliability issues and solutions, Applications.

UNIT - V

NAND Flash Memory Technology: Overview of NAND EEPROM, NAND Cell operation, NAND array architecture and operation, Program threshold control and program V_t Spread reduction, Process and scaling issues, Key Circuits and Circuit technology interactions, Multilevel NAND.

UNIT – VI

DINOR Flash Memory Technology: DINOR operation and array architecture, DINOR Technology features, DINOR Circuit for low voltage operation, Background operation function, P-Channel DINOR architecture.

UNIT –VII

P-Channel Flash Memory Technology: Introduction, Device structure, Operations of P-Channel flash, Evolution of P-Channel flash.

UNIT -VIII

Embedded Flash memory: Embedded Flash versus Stand alone flash memory, Embedded flash memory applications, Embedded flash memory cells, Embedded flash memory design.

Text Books:

1. J. Brewer and M. Gill, "Nonvolatile memory technologies with emphasis on Flash," IEEE press series on microelectronic systems, Wiley – Interscience, 2008.
2. T. Y. Tseng and S. M. Sze, "Nonvolatile Memories-Materials, Devices and Applications," American Scientific Publishers, Vol. 1 & 2, 2012.

Reference Books:

1. S. Lai, "Flash Memories: Successes and Challenges, IBM Journal of Res. & Dev. Vol. 52, p529, 2008.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th 4** **C 4**

(9D55202) Real Time Operating Systems

UNIT - I

Brief Review of Unix Operating Systems: Unix Kernel – File system, Concepts of – Process, Concurrent Execution & Interrupts, Process Management – forks & execution, Programming with system calls, Process Scheduling, Shell programming and filters.

UNIT - II

Portable Operating System Interface (POSIX) – IEEE Standard 1003.13 & POSIX real time Profile, POSIX versus traditional Unix signals, overheads and timing predictability.

UNIT - III

Hard versus Soft Real-time systems – examples, Jobs & Processors, Hard and Soft timing constraints, Hard Real-time systems, Soft Real-time systems.

UNIT - IV

Classical Uniprocessor Scheduling Algorithms – RMS, Preemptive EDF, Allowing for Preemptive and Exclusion Condition.

UNIT V

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS. Real-time System Concepts, RTOS Kernel & Issues in Multitasking – Task Assignment, Task Priorities, Scheduling.

UNIT - VI

Intertask Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks, Critical Section – Reentrant Functions, Inter-process Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

UNIT -VII

VxWorks – POSIX Real Time Extensions, timeout features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues, Memory Management – Virtual to Physical Address Mapping.

UNIT - VIII

Debugging Tools and Cross Development Environment – Software Logic Analyzers, ICEs, Comparison of RTOS – VxWorks, μC/OS-II and RT Linux for Embedded Applications.

Text Books:

1. Jane W. S. Liu, "Real Time Systems, Pearson Education," Asia, 2001.
2. Betcnhof, D.R., "Programming with POSIX threads," Addison - Wesley Longman, 1997.
3. C.M.Krishna and G.Shin, "Real Time Systems," McGraw-Hill, 1997.

Reference Books:

1. Jean.J.Labrosse, MicroC/OS-II, The CMP Books.
2. Wind River Systems, VxWorks Programmers Guide, Wind River Systems Inc.1997.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th 4** **C 4**

(12D68202) DSP Architectures and Applications

UNIT – I

Fundamentals of Programmable DSPs: Multiplier and multiplier accumulator – Modified bus structures and Memory access in P-DSPs – Multiple access memory.

UNIT – II

Multiport memory – VLIW architecture – Pipelining – Special addressing modes in P-DSPs – On chip peripherals.

UNIT – III

TMS320C5X Processor: Architecture – Assembly language syntax – Addressing modes – Assembly language instructions – Pipeline structure, operation.

UNIT – IV

Block diagram of DSP (TMS320C5X) starter kit – Application programs for processing real time signals.

UNIT – V

TMS320C3X Processor: Architecture – Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation.

UNIT – VI

Block diagram of DSP (TMS320C3X) starter kit – Application programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design.

UNIT – VII

ADSP Processors: Architecture of ADSP-21XX and ADSP-210XX series of DSP processors – Addressing modes and assembly language instructions – Application programs – Filter design, FFT calculation.

UNIT – VIII

Advanced Processors: Architecture of TMS320C54X: Pipeline operation, Code Composure studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors – Applications.

Text Books:

1. B. Venkataramani and M. Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications," Tata McGraw Hill, New Delhi, 2003.
2. User guides: Texas Instrumentation, Analog Devices, Motorola.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th 4** **C 4**

(12D68203) ASIC Design

UNIT – I

Introduction to ASICS, CMOS logic and ASIC library design: Types of ASICs – Design flow – CMOS transistors, CMOS design rules – Combinational logic cell.

UNIT - II

Sequential logic cell – Data path logic cell – Transistors as resistors – Transistor parasitic capacitance – Logical effort – Library cell design – Library architecture.

UNIT –III

Programmable ASICs, Programmable ASIC logic cells and Programmable ASIC logic I/O cells: Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT.

UNIT - IV

Xilinx LCA – Altera FLEX – Altera MAX DC and AC inputs and ouputs – Clock and power inputs – Xilinx I/O blocks.

UNIT – V

Programmable ASIC interconnect, Programmable ASIC design software and low level design entry: Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX – Design systems.

UNIT - VI

Logic Synthesis – Half gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

UNIT – VII

Logic Synthesis, Simulation and Testing: Verilog and logic synthesis – VHDL and logic synthesis – types of simulation – boundary scan test – fault simulation – automatic test pattern generation.

UNIT – VIII

ASIC Construction, floor planning, placement and routing: System partition – FPGA partitioning – partitioning methods – floor planning – placement – Physical design flow – Global routing – Detailed routing – Special routing – Circuit extraction – DRC.

Text Books:

1. M. J. S. Smith, "Application Specific Integrated Circuits," Addition – Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, " From ASICs to SOCs: A practical Approach," Prentice Hall PTR, 2003.
3. Wayne Wolf, "FPGA based System Design," Prentice Hall PTR, 2004.

Reference Books:

1. R. Rajsuman, "System - on – a – chip design and Test Santa Clara, CA," Artech House Publishers, 2000.
2. F. Nekoogar, "Timing Verification of Application Specific Integrated Circuits (ASICs)," Prentice Hall PTR, 1999.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th** **C**

4 **4**

(12D68204) Software Defined Radio (SDR)
ELECTIVES - II

UNIT – I

Introduction to Software Radio Concepts: The need for Software radios and its definition, Characteristics and benefits of Software radio, Design principles of a software radio.

UNIT – II

Radio Frequency Implementation Issues: Purpose of RF front – end, Dynamic range, RF receiver front – end topologies, Enhanced flexibility of the RF chain with software radios, Importance of the components to overall performance, Transmitter architectures and their issues, Noise and distortion in the RF chain, ADC & DAC distortion.

UNIT – III

Pre-distortion, Flexible RF systems using micro-electromechanical systems, Multirate Signal Processing in SDR: Sample rate conversion principles, Polyphase filters, Digital filter banks, Timing recovery in digital receivers using multirate digital filters.

UNIT – IV

Digital Generation of Signals: Introduction, Comparison of direct digital synthesis with analog signal synthesis, Approaches to direct digital synthesis, Analysis of spurious signals, Spurious components due to periodic jitter, Bandpass signal generation, Performance of direct digital synthesis systems, Hybrid DDS – PLL Systems, Applications of direct digital synthesis, Generation of random sequences, ROM compression techniques.

UNIT – V

Smart Antennas: Introduction, Vector channel modelling, Benefits of smart antennas, Structures for beamforming systems, Smart antenna algorithms, Diversity and Space time adaptive signal processing, Algorithms for transmit STAP.

UNIT – VI

Hardware implementation of smart antennas, Array calibration, Digital Hardware Choices, Key hardware elements, DSP processors, FPGAs, Power measurement issues.

UNIT – VII

Object oriented Representation of Radios and Network: Networks, Object –oriented programming, Object brokers, Mobile application environments, Joint Tactical radio system.

UNIT – VIII

Case Studies in Software Radio Design: SPEAKeasy, JTRS, Wireless Information transfer system, SDR-3000 digital transceiver subsystem, Spectrum Ware, Brief introduction to Cognitive Networking.

Text Books:

1. Jeffrey Hugh Reed, "Software Radio: A Modern Approach to Radio Engineering," Prentice Hall Professional, 2002.
2. Paul Burns, "Software Defined Radio for 3G," Artech House, 2002.

Reference Books:

1. Tony J Rouphael, "RF and DSP for SDR," Elsevier Newnes Press, 2008.

2. P. Kenington, "RF and Baseband Techniques for Software Defined Radio," Artech House, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th 4** **C 4**

(12D68205) VLSI Signal Processing
ELECTIVES - II

UNIT - I

Introduction To DSP Systems -Typical DSP algorithms - Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT- II

Retiming - definitions and properties - Unfolding – algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT - III

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition.

UNIT - IV

Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT - V

Scaling and round-off noise - scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined first-order filters.

UNIT - VI

Bit-Level Arithmetic Architectures - parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement.

UNIT - VII

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining-synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol;

UNIT - VIII

Programming Digital Signal Processors – general architecture with important features, Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

Text Books:

1. Keshab K.Parhi, “VLSI Digital Signal Processing systems, Design and implementation,” Wiley, Inter Science, 1999.
2. Gary Yeap, “Practical Low Power Digital VLSI Design,” Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing,” Mc Graw-Hill, 1994.

Reference Books:

1. S.Y. Kung, H.J. White House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
2. Jose E. France, Yannis Tsividis, “Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing,” Prentice Hall, 1994.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **Th** **C**

4 **4**

(12D68206) Design and Testability
ELECTIVES - II

UNIT – I

Physical defects and their modelling: Struck at faults, Bridging faults, Fault collapsing, Fault simulation: deductive, parallel and concurrent, critical path tracing.

UNIT – II

Test generation for Combinational Circuits: D – Algorithm, Boolean difference, PODEM, and ATPG.

UNIT – III

Random, Exhaustive and Weighted: Random Test pattern generations, Aliasing and its effect on fault coverage.

UNIT – IV

PLA Testing: Cross point Fault model, Test generation.

UNIT – V

Memory Testing: Permanent intermittent and pattern sensitive faults, Delay faults and Hazards, Test generation techniques.

UNIT – VI

Test generation for Sequential Circuits.

UNIT – VII

Scan Design, Scan path and LSSD, BILBO, Concept of redundancy, Spatial redundancy, Time redundancy.

UNIT – VIII

Recent trends in VLSI testing: Genetic Algorithms, Parallel Algorithms, Neural Networks, Nano Scale Testing.

Text Books:

1. Stanley L. Hurst, "VLSI Testing: Digtal and mixed analogue digital techniques," Inspec/IEE, 1999.
2. Laung Terng Wang, Cheng Wen Wu, Xiaaqing Wen, "VLSI Test Principles and Architectures: Design and Testability."
3. Gordon Russell, "Advanced Simulation and Test Methodologies for VLSI Design."

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. II SEM (VLSI & ES) **L C**

3 2

(12D68207) FPGA DESIGN LABORATORY

Note: i. ***All the experiments are to be carried out independently by each student, with different specifications***:

ii. ***At least 15 experiments are to be carried out***.

1. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after that Simulations are to be verified using FPGA/CPLD blocks from different commercially available products on:

   Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
   Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

2. Experiments on Digital Signal Processors.
3. Mini projects on RTOS