



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
Academic Regulations For The Award Of Full Time M.Tech. P.G. Degree
(WITH EFFECT FROM THE ACADEMIC YEAR 2009-10)

The Jawaharlal Nehru Technological University Anantapur shall confer M.Tech. Post Graduate degree to candidates who are admitted to the Master of Technology Programs and fulfill all the requirements for the award of the degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the University for each programme, from time to time.

Admissions shall be made either on the basis of merit rank obtained by the qualified candidates at an Entrance Test conducted by the University or on the basis of GATE / PGECET score, subject to reservations prescribed by the University or Government policies from time to time.

2.0 COURSE WORK:

- 2.1 A Candidate after securing admission must pursue the M.Tech. course of study for Four semesters duration.
- 2.2 Each semester shall be of 20 weeks duration including all examinations.
- 2.3 A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

3.0 ATTENDANCE:

- 3.1 A candidate shall be deemed to have eligibility to write end semester examinations if he has put in at least 75% of attendance on cumulative basis of all subjects/courses in the semester.
- 3.2 Condonation of shortage of attendance up to 10% i.e., from 65% and above and less than 75% may be given by the college on the recommendation of the Principal.
- 3.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.
- 3.4 If the candidate does not satisfy the attendance requirement he is detained for want of attendance and shall reregister for that semester. He / she shall not be promoted to the next semester.

4.0. EVALUATION:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

4.1 For the theory subjects 60% of the marks will be for the External End Examination. While 40% of the marks will be for Internal Evaluation, based on the better of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (I-IV units) and another immediately after the completion of instruction (V-VIII) units with Three questions to be answered out of four in 2hours, evaluated* for 40 marks.

*Note: All the Questions shall be of equal weightage of 10 marks and the marks obtained for 3questions shall be extrapolated to 40 marks, any fraction rounded off to the next higher mark

4.2 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day to day performance.

4.3 For Seminar there will be an internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts at the end of IV semester instruction.

4.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

4.5 In case the candidate does not secure the minimum academic requirement in any of the subjects (as specified in 4.4.) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

5.0 RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL EVALUATION MARKS:

Following are the conditions to avail the benefit of improvement of internal evaluation marks.

5.1 The candidate should have completed the course work and obtained examinations results for I & II semesters.

5.2 He should have passed all the subjects for which the Internal evaluation marks secured are more than 50%.

5.3 Out of the subjects the candidate has failed in the examination due to Internal evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

5.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

5.5 For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the

Registrar, JNTUA payable at Anantapur along with the requisition through the Principal of the respective college.

- 5.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

6.0 EVALUATION OF PROJECT WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the college/ institute.

- 6.1 Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Sem)
- 6.2 An Internal Departmental Committee (I.D.C) consisting of HOD, Supervisor and one internal senior expert shall monitor the progress of the project work.
- 6.3 The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest and one calendar year from the date of registration for the project work. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.
- 6.4 The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.
- 6.5 A candidate shall be allowed to submit the thesis / dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva-voce examination may be conducted once in two months for all the candidates submitted during that period.
- 6.6 Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor & HOD shall be presented to the H.OD. One copy is to be forwarded to the University and one copy to be sent to the examiner.
- 6.7 The college shall submit a panel of three experts for a maximum of 5 students at a time. However, the thesis / dissertation will be adjudicated by one examiner nominated by the University.
- 6.8 If the report of the examiner is favorable viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis / dissertation. The board shall jointly report candidates work as:
- | | | |
|----|------------------|---------|
| 1. | Very Good | Grade A |
| 2. | Good | Grade B |
| 3. | Satisfactory | Grade C |
| 4. | Not satisfactory | Grade D |

If the report of the viva-voce is not satisfactory (Grade D) the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

7.0 AWARD OF DEGREE AND CLASS:

A candidate shall be eligible for the award of respective degree if he satisfies the minimum academic requirements in every subject and secures 'satisfactory' or higher grade report on his thesis/dissertation and viva-voce. Based on overall percentage of marks obtained, the following class is awarded.

First class with Distinction:	70% or more
First class	below 70% but not less than 60%
Second class	below 60% but not less than 50%

8.0 WITH – HOLDING OF RESULTS:

If the candidate has not paid dues to the university or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed/ promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

Candidates who have discontinued or have been detained for want of attendance or who have failed after having undergone the course in earlier regulations and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to 4.5 and 2.3 sections. Whereas they continue to be in the academic regulations they were first admitted.

10.0 GENERAL:

- i. **The academic regulations should be read as a whole for purpose of any interpretation.**
- ii. **Disciplinary action for Malpractice / improper conduct in examinations is appended.**
- iii. **There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.**
- iv. **Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".**
- v. **In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.**
- vi. **The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.**

**RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT
IN EXAMINATIONS**

	Nature of Malpractices/Improper conduct	Punishment
	<i>If the candidate</i>	
1.	<p>(a) Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)</p>	Expulsion from the examination hall and cancellation of the performance in that subject only.
	<p>(b) Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.</p>	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
6.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.

7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
8.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions : (if the squad reports that the college is also involved in encouraging malpractices)
 - (i) A show cause notice shall be issued to the college.
 - (ii) Impose a suitable fine on the college.
 - (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

**Course Structure and Syllabus for M.Tech. Embedded Systems
for affiliated Engineering Colleges, 2009-10**

I YEAR I SEMESTER

S. No	Course code	Subject	Theory	Lab.	Credits
1.	9D55101	Advanced DSP & Applications	4		4
2.	9D06102	Embedded System Concepts	4		4
3.	9D06103	Advanced Computer Architecture	4		4
4.	9D55104	Micro Controllers & Interfacing	4		4
5.	9D55105	Operating Systems	4		4
6.		ELECTIVE I	4		4
	9D57103a	a. Digital IC Design			
	9D57101b	b. VLSI Technology			
	9D55106c	c. Algorithms for VLSI Design Automation			
7.	9D55107	Microcontrollers & Interfacing Lab		3	2
		contact periods/week	24	3	
			Total	27	26

I YEAR II SEMESTER

S. No	Course code	Subject	Theory	Lab.	Credits
1.	9D55201	Testing & Testability	4		4
2.	9D55202	Real Time Operating Systems	4		4
3.	9D55203	Hardware Software Co-design	4		4
4.	9D55204	FPGA Architecture & Applications	4		4
5.	9D55205	Cryptography & Network Security	4		4
6.		ELECTIVE II	4		4
	9D55206a	a. Radio Frequency Identification			
	9D55206b	b. Micro Electromechanical Systems			
	9D55206c	c. Expert Systems			
7.	9D55207	RTOS & FPGA Lab		3	2
		contact periods/week	24	3	
			Total 27		26

II YEAR (III & IV Semesters)

S. No	Course code	Subject		credits
1	9D55401	Seminar		2
2	9D55402	Project work		16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. I SEMESTER (EMBEDDED SYSTEMS)

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(9D55101) ADVANCED DSP & APPLICATIONS**UNIT I**

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Simple digital filters, Complementary Transfer Functions, Inverse Systems, System identification, Digital Two-Pairs, Algebraic Stability Test.

UNIT II

DIGITAL FILTER STRUCTURE AND DESIGN: All pass filters, Tunable IIR Digital filter, IIR tapped Cascaded Lattice Structures, FIR Cascaded lattice Structures, Parallel All pass realization of IIR Transfer Functions, State Space Structures, Polyphase Structures, Digital Sine-Cosine generator,

UNIT III

Computational Complexity of Digital filter Structures, Design of IIR filter using pade' approximation, Least square design methods, Design of computationally Efficient FIR Filters.

UNIT IV

DSP ALGORITHMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT V & VI

ANALYSIS OF FINITE WORD LENGTH EFFECTS: The Quantization Process and errors, Quantization of fixed-point Numbers, Analysis of Coefficient quantization effects, A/D conversion Noise Analysis, Analysis of Arithmetic Round of errors, Dynamic range scaling, Signal to Noise ratio in Low-order IIR Filters, Low sensitivity Digital filters, Reduction of Product Round off Errors using error feedback, Limit cycle in IIR Digital filters, Round of errors in FFT algorithms.

UNIT VII

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Nonstationary Signals, Musical Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete -Time Analytic Signal generation.

UNIT VIII

Current Trends in Digital Signal Processors / DSP Controllers - Architecture - DSP Applications.

TEXT BOOKS:

1. Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications
2. Digital Signal Processing Principles, Algorithms, Applications By J G Proakis, D G Manolakis, PHI.
3. Discrete-Time Signal Processing by A V Oppenheim, R W Schaffer, Pearson Education Asia.

REFERENCES:

1. Naim Dahnoun, "Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform", 1st Edition.
2. T.J. Terrel and Lik-Kwan Shark, "Digital Signal Processing-A Student Guide", 1st Edition, MACMILLAN PRESS Ltd.
3. David J Defatta J, Lucas Joseph G & Hodkiss William S, "Digital Signal Processing: A System Design Approach", 1st Edition, John Wiley.
4. Rulph Chassaing, "DSP Applications using 'C' and the TMS320C6X DSK", 1st Edition.
5. Andrew Bateman, Warren Yates, "Digital Signal Processing Design", 1st Edition.
6. John G Proakis, Dimitris G Manolakis, "Introduction to Digital Signal Processing", 1st Edition.
7. Kreig Marven & Gillian Ewers, "A Simple approach to Digital Signal processing", 1st Edition, Wiely Interscience.
8. JAMES H. McClellan, Ronald Schaffer and Mark A. Yoder, "DSP FIRST - A Multimedia Approach", 1st Edition, Prentice Hall.
9. Oppenheim A.V and Schaffer R.W, "Digital Signal Processing", 1st Edition, PH.

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M.Tech. I SEMESTER (EMBEDDED SYSTEMS)

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(9D06102) EMBEDDED SYSTEM CONCEPTS

UNIT I- INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

UNIT II- EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacing: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III- SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

UNIT IV- EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT V- RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

UNIT VI- INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VII- SYSTEM DESIGN TECHNIQUES:

Design methodologies, requirement analysis, specifications, system analysis and architecture design

UNIT VIII- DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes..

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D.Givargis, John Willey, 2002

M.Tech. I SEMESTER (EMBEDDED SYSTEMS)**Th C
4 4****(9D06103) ADVANCED COMPUTER ARCHITECTURE**

UNIT I-FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost-measuring and reporting performance quantitative principles of computer design.

UNIT II-INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT III-INSTRUCTION LEVEL PARALLELISM (ILP): over coming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

UNIT IV-ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W versus S.W solutions

UNIT V-MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT VI-MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT VII-STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT VIII-INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

TEXT BOOKS:

1. John. Hennessy & David A. Patterson Morgan Kufmann, "Computer Architecture A quantitative approach", 3rd edition (An Imprint of Elsevier)

REFERENCES:

1. Kai Hwang and A. Briggs, "Computer Architecture and parallel Processing", International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

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M.Tech. I SEMESTER (EMBEDDED SYSTEMS)

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(9D55104) MICROCONTROLLERS & INTERFACING

UNIT I- INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples.

UNIT II- 8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT III- MOTOROLA 68HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system.

UNIT IV-Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT V- PIC MICROCONTROLLERS: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, I²C bus, ADC, UART, PIC family parts.

UNIT VI- MICROCONTROLLER INTERFACING: 8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT VII- INTERRUPT SYNCHRONIZATION: Interrupt vectors & priority, external interrupt design. Serial I/O Devices RS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial Communication Controller.

UNIT VIII

CASE STUDIES: Design of Embedded Systems using the micro controller 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

TEXT BOOKS:

1. M.A. Mazadi & J.G. Mazidi, “The 8051 Micro Controller & Embedded Systems”, Pearson Education. Asia (2000).
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education.
3. Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.

REFERENCES:

1. 8-bit Embedded Controllers, INTEL Corporation 1990.
2. John B. Peatman, “Designing with PIC Microcontrollers”, Pearson Education Inc, India, 2005.

M.Tech. I SEMESTER (EMBEDDED SYSTEMS)

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(9D55105) OPERATING SYSTEMS

UNIT I-INTRODUCTION: Operating system definition, Objective and functions, types, different parts, Structure of operating system, trends- parallel computing, distributed computing; Open systems, Hardware, software, firmware

UNIT II-PROCESS SCHEDULING: Definition of a process; process states, transitions, process control, suspend and process, interrupt processing, nucleus of an operating system; parallel processing; Mutual exclusion, Critical Section; Solution of mutual exclusion; Semaphores; Deadlock- occurrence, prevention, detection and recovery;

UNIT III-STORAGE MANAGEMENT: Storage organization, management strategies, hierarchy; virtual storage, paging, segmentation.

UNIT IV-FILE SYSTEM MANAGEMENT: File system (function of a file system)- data hierarchy, blocking and buffering, file organization, queued and basic access methods, backup and recovery;

UNIT V-I/O MANAGEMENT: (functions of I/O management subsystem), Distributed computing- OSI view, OSI network management, MAP, TOP, GOSIP, TCP/IP;

UNIT VI-OS SECURITY: Requirements, external security, operational security, surveillance, threat monitoring; Introduction to Cryptography.

UNIT VII & VIII-CASE STUDIES: UNIX- Shell, Kernel, File System, Process Management, Memory Management, I/O System, Distributed UNIX; Example of operating system-MS-DOS, Windows, OS/2, Apple Macintosh & Linux.

TEXT BOOKS:

1. Dietal H.M , “An Introduction to OS” Pearson Education pvt.Ltd/PHI New Delhi, 12th Indian Reprint 2003.
2. Andrew S.Tanenbaum, “Modern OS”PHI Pearson Education pvt.Ltd New Delhi, 3rd Indian Reprint 2004.
3. Silberschatz . A, Galvin.p and Gagne.G, “Operating System Concepts”, John Wiley and Sons. Singapore,2002.

REFERENCES:

1. William Stallings, ”Operating Systems”, Pearson Education pvt.Ltd.
2. D.M. Dhamdhere, ”Operating Systems – A Concept Approach”, Tata McGraw Hill, 2003.

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M.Tech. I SEMESTER (EMBEDDED SYSTEMS)

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**ELECTIVE I
(9D57103a) DIGITAL IC DESIGN**

UNIT I-CMOS inverters -static and dynamic characteristics.

UNIT II -Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT III-Method of Logical Effort for transistor sizing -power consumption in CMOS gates-Low power CMOS design.

UNIT IV -Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT V -Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

UNIT VI&VII -LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load.

UNIT VIII-SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999
2. Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1997
3. Eugene D Fabricus, "Introduction to VLSI Design,"McGraw Hill Intl Edition.1990

REFERENCES:

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000
2. Neil H E West and Kamran Eshranghian,"Principles of CMOS VLSI Design: A System Perspective", Addison-Wesley 2nd Edition,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation". New York: IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, "Analysis and Design of Digital Integrated Circuits", Third Edition, McGraw-Hill, 2004.

M.Tech. I SEMESTER (EMBEDDED SYSTEMS)

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**ELECTIVE I
(9D57101b) VLSI TECHNOLOGY**

UNIT I-REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology trends and projections.

UNIT II-BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds relationships, Threshold voltage V_t , G_m , G_{ds} and W_o , Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd} , MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT III-LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT IV-LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT V-COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network Delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT VI-SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VII-FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High level Synthesis, Architecture for Low Power, SOCs and Embedded Cpus, Architecture Testing.

UNIT VIII-INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware/Software Co-Design, Chip Design Methodologies- a Simple Design Example.

TEXT BOOKS:

1. K. Eshraghian et . al(3 authors), "Essentials of VLSI Circuits and Systems", PHI of India Ltd., 2005
2. Wayne Wolf , "Modern VLSI Design", 3/E, Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. N.H.E Weste, K.Eshraghian, "Principals of CMOS Design", Adison Wesley, 2nd Edition.
2. Fabricius, "Introduction to VLSI Design", MGH International Edition, 1990.
3. Baker, Li Boyce, "CMOS Circuit Design, Layout and Simulation", PHI, 2004.

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ELECTIVE I**(9D55106c) ALGORITHMS FOR VLSI DESIGN AUTOMATION**

UNIT I-PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II-GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III-Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV-MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V-LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI-HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VII-PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VIII-PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Hill&Peterson,"Computer Aided Logical Design with Emphasis on VLSI",Wiley, 1993
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition, 1998

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(9D55107) MICROCONTROLLERS & INTERFACING LAB

ASSEMBLY:

1. Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2. A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7. Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.
3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.
4. Stepper Motor Control using Microcontroller.

Use Microcontrollers for the following Experiments.

INTERFACING:

5. Elevator Interface.
6. Key Board Interface.
7. LED Interface.
8. Temperature Sensor.
9. SORT RTO'S on to 89c51 Board.
10. Sample the Signal using ADC and Reconstruct by using DAC.

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(9D55201) TESTING & TESTABILITY**UNIT I-INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT)**

FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II-FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT III-TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT IV&V-DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT VI-BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT VII-MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

UNIT VIII-BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.

REFERENCES:

1. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
2. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

M.Tech. II SEMESTER (EMBEDDED SYSTEMS)**Th C**
4 4**(9D55202) REAL TIME OPERATING SYSTEMS**

UNIT I-INTRODUCTION TO UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT II&III-REAL TIME SYSTEMS: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT IV-APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

UNIT V-OPERATING SYSTEMS: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT VI-FAULT TOLERANCE TECHNIQUES: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

UNIT VII-CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT VIII-RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

1. Richard Stevens, “Advanced Unix Programming”.
2. Jane W.S. Liu, “Real Time Systems”, Pearson Education.
3. C.M.Krishna, KANG G. Shin, “Real Time Systems”, McGraw.Hill

REFERENCES:

1. VxWorks Programmers Guide
2. www.tidp.org
3. www.kernel.org
4. <http://www.xml.com/ldd/chapter/book>

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(9D55203) HARDWARE SOFTWARE CO- DESIGN

UNIT I-CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

UNIT II-CO- SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT III-PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT IV-TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT V-COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT VI-DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT VII-LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages,

UNIT VIII-LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / software co- design Principles and Practice”, Springer, 2009.
2. Kluwer, “Hardware / software co- design Principles and Practice”, academic publishers,2002.

M.Tech. II SEMESTER (EMBEDDED SYSTEMS)**Th C
4 4****(9D55204) FPGA ARCHITECTURE & APPLICATIONS****UNIT I**

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD’s – CPLD (Mach 1 To 5); Cypress FLASH 370 Device Technology, Lattice Plsi’s Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT III

CASE STUDIES: Xilinx XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT & T – ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s – ACT-1,2,3 and Their Speed Performance.

UNIT IV

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT V

REALIZATION OF STATE MACHINE: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT VI& VII

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT VIII

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: Using Mentor Graphics EDA Tool (“FPGA Advantage”) – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS/ REFERENCES:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publicatgions,1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.

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(9D55205) CRYPTOGRAPHY & NETWORK SECURITY

UNIT I-SYMMETRIC CIPHERS: Overview, classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

UNIT II-PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS: Introduction to Number Theory, Public-Key Cryptography and RSA-Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT III-NETWORK SECURITY PRACTICE: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT IV-SYSTEM SECURITY: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

UNIT V-WIRELESS SECURITY: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT VI-SECURE NETWORKING THREATS: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT VII-ENCRYPTION TECHNIQUES: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT VIII-DESIGNING SECURE NETWORKS: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, The Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations, ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. William Stallings, “Cryptography and Network Security – Principles And Practices”, Pearson Education, 3rd Edition, 2003.
2. Sean Convery, “ Network Security Architectures, Published by Cisco Press, First Ed.2004.

REFERENCES:

1. Atul Kahate, “Cryptography and Network Security”, Tata McGraw Hill, 2003.
2. Bruce Schneier, “Applied Cryptography”, John Wiley and Sons Inc, 2001.
3. Stewart S. Miller, “Wi-Fi Security”, McGraw Hill, 2003.
4. Charles B. Pfleeger, Shari Lawrence Pfleeger, “Security In Computing”, 3rd Edition, Pearson Education, 2003.
5. Jeff Crume, “Inside Internet Security” Addison Wesley, 2005.

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ELECTIVE II
(9D55206a) RADIO FREQUENCY IDENTIFICATION

UNIT I

UNDERSTANDING RFID TECHNOLOGY: Introduction, RFID Technology, The Elements of an RFID system, Coupling, Range, and Penetration, RFID Applications, VeriChip and Mark of the Beast.

UNIT II&III

A HISTORY OF THE EPC: Introduction, The Distributed Intelligent Systems Center, Meanwhile, at Procter & Gamble, “Low-Cost” RFID Protocols, “Low-cost” Manufacturing, The Software and the Network, Privacy, Harnessing the Juggernaut, The Six Auto-ID Labs, The Evolution of the Industry, The Creation of EPC global.

UNIT IV&V

RFID AND GLOBAL PRIVACY POLICY: Introduction, Definitions of Privacy, Definitions of Personal Information, History of Current Privacy Paradigm, Mapping the RFID Discovery process, Functions and Responsibilities for chips, Readers, and Owners, Privacy as a Fundamental Human Right, Constitutional Rights.

UNIT VI&VII

RFID, PRIVACY, AND REGULATION: Introduction, Understanding RFID’s Privacy Threats. RFID and the United States Regulatory Landscape: Introduction, Current State of RFID Policy, Individuals, Business, Government, Miscellaneous, Integrity and Security of the System, Government Access, Health Impact, Labor Impact

UNIT VIII

APPLICATIONS: RFID Payments at ExxonMobil, Exxon Mobil Corporation, Transforming the Battlefield with RFID, Logistics and the Military, RFID in the Pharmacy, CVS and Auto-ID, Project Jump Start, RFID in the Store.

TEXT BOOKS:

1. Simson Garfinkel and Beth Rosenberg, “RFID Applications, Security, and privacy”, Pearson Education
2. Steven Shepard, “Radio Frequency Identification”, First edition, McGraw-Hill Professional.

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(ELECTIVE II)

(9D55206b) MICRO ELECTROMECHANICAL SYSTEMS

UNIT I&II-INTRODUCTION, BASIC STRUCTURES OF MEM DEVICES: (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro Electromechanical Systems (MEMS) to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatability of MEMS from the point of Power Dissipation, Leakage etc.

UNIT III-REVIEW OF MECHANICAL CONCEPTS: Stress, Strain, Bending Moment, Deflection Curve. Differential Equations Describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed Beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with Voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT IV-TWO TERMINAL MEMS: Capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM Structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT V&VI-MEM CIRCUITS & STRUCTURES FOR SIMPLE GATES: AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT VII&VIII-MEM TECHNOLOGIES: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

TEXT BOOKS:

1. Gabriel.M.Review, “R.F. MEMS Theory, Design and Technology”, John Wiley & Sons, 2003.
2. Thimo Shenko, ”Strength of Materials”, CBS Publishers & Distributors., 2000.
3. Ristic L. (Ed.), “Sensor Technology and Devices”, Artech House, London 1994.
4. Servey E.Lyshevski, “MEMS and NEMS, Systems Devices; and Structures”, CRC Press, 2002.

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ELECTIVE II
(9D55206c) EXPERT SYSTEMS
UNIT I

KNOWLEDGE REPRESENTATION AND ISSUES: Notational systems: Trees, graphs, hierarchies, propositional and predicate logics, frames, semantics networks, constraints, conceptual dependencies, database, knowledge discovery in databases (KDD).

UNIT II

SEARCH: State-space representations, Depth-first, breadth-first, heuristic search, Planning and game playing, Genetic algorithms.

UNIT III&IV

LOGICAL REASONING AND PROBABILISTIC REASONING: Predicate, Calculus resolution, completeness, and strategies, Unification, Prolog, monotonic and non-monotonic reasoning, Probabilistic inference networks, Fuzzy inference rules, Bayesian rules. Dempster-Shafer Calculus.

UNIT V&VI

LEARNING AND COMMON SENSE REASONING: Robot actions, strips, triangle tables, case based reasoning, spatial and temporal formalisms. Knowledge acquisition, classification rules, self directed systems.

UNIT VII&VIII

NEURAL NETWORKS AND EXPERT SYSTEMS: Principles, biological analogies, Training (techniques and errors), Recognition, Expert Systems, Organization, tools, limits, examples.

TEXT BOOKS:

1. Charniak .E,And McDermott .D., "Intoduction to Artificial intelligence", Adiison-Wesley, 1987
2. Giarratano.J.,And Riley G., "Expert Systems principles an Programming" PWS-KENT,1989

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(9D55207) RTOS & FPGA Lab

1. RTOS System solution & tools
2. Testing RTOS Environment and System Programming.
 - a) Keil Tools
 - b) RTOS System Solutions with Tornado tools.
3. Embedded DSP based System Designing.
 - a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
 - b) Analog DSP tool kit.
4. Synthesis of the designs made using “VHDL / VERILOG and Mixed Design (VHDL & Verilog)” after Simulation are to be verified using FPGA/CPLD blocks from different commercially available products on:
 - a). Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
 - b) Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

NOTE: Required Software Tools for FPGA:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

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(9D55401) SEMINAR

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(9D55402) PROJECT WORK

The Project Work should be on a contemporary topic relevant to the core subjects of the course. It should be original work of the candidate.
